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A Study of Class C Applications of Power Transistors at High and Very High Frequencies

by
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Technical Report No. 713-1

Prepared under
Signal Corps Contract DA 36-039 SC-87300

SYSTEMS TECHNIQUES LABORATORY

STANFORD ELECTRONICS LABORATORIES

STANFORD UNIVERSITY · STANFORD, CALIFORNIA

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ABSTRACT

The operation of power transistors in Class C amplifiers at high and very high frequencies is considered. At the lower end of this frequency range, static characteristics are an appropriate basis for the analysis.

Two analytic methods and one graphical method of analysis are developed for the nonsaturating case. These methods present the output power, efficiency, and power gain as functions of the operating conditions. By plotting these quantities as contours on peak collector current - flow angle coordinates it is possible to optimize the design.

Operation into saturation is examined and equations developed for this case. It is shown that significantly better results can be obtained for this mode of operation.

Very high frequency operation is next examined. The various factors affecting such operation are explained and an approximate analysis developed based on an analogy to an RC transmission line.

A new method of simulation of a transistor is presented based on the excess-charge-density two-lump model. It is shown how this method can be applied to simulate operation in saturation and to account for the major nonlinearities and two-dimensional effects present in a transistor. Test results are presented for a single two-lump approximation for a vhf power transistor operating as a Class C amplifier.

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ILLUSTRATIONS (Cont'd)

ILLUSTRATIONS (Cont'd)

LIST OF SYMBOLS

A	value of v_B for $v_C = 0$, a function of i_C
A_E	constant of proportionality in emitter depletion capacitance-applied voltage equation
B	$\partial v_B / \partial v_C$, a function of i_C
BV_{CES}	maximum allowable collector-emitter reverse voltage with emitter base shorted
C	shunt capacitance of RC line
C_{CE}	portion of collector depletion capacitance not under the emitter
C_{CI}	portion of collector depletion capacitance under the emitter
C_E	emitter depletion capacitance
D	a function of γ, g_{mo}, V_{CC}, and $V_{C,min}$
E_C	collector efficiency
f	frequency
f_1	a function of $V_{C,min}$, $I_{C,max}$, $\omega\tau$, $\omega\tau'$
f_L	cutoff frequency of transistor base line with load signal
F_L	cutoff frequency of transistor base line with no load signal
g_{mc}	collector storance amplifier transconductance
g_{md}	diffusance amplifier transconductance
g_{me}	emitter storance amplifier transconductance
g_{mo}	zero collector voltage transconductance
G	power gain
G_1	coefficient which approximates i_B by a power function
H_1	combinance, emitter side
H_2	combinance, collector side
H_D	diffusance
i_B	total instantaneous base current
i'_B	approximation to base charging current

LIST OF SYMBOLS (Cont'd)

i_C	total instantaneous collector current
i_{CR}	collector recombination current
i_{CS}	collector storance current
i_D	diffusance current
i_E	emitter current
i_{ER}	emitter recombination current
i_{ES}	emitter storance current
I_{B1}	fundamental component of base current
$I_{B,max}$	peak base current
$I'_{B,max}$	the peak base current which would flow except for saturation
I_{BDC}	dc component of base current
I_{C1}	fundamental component of collector current
$I_{C,max}$	peak collector current
$I'_{C,max}$	the peak collector current which would flow except for saturation
I_{CDC}	dc component of collector current
I_{sat}	saturation current of actual diode
I_{S1}	emitter diode saturation current
I_{S2}	collector diode saturation current
k	Boltzmann's constant
$K_1(\omega\tau)$, $K_2(\omega\tau)$	particular functions of $\omega\tau$
$K_3(\omega\tau,\alpha_i)$	a function of $\omega\tau$ and α_i
$K_4(\omega\tau,D)$, $K_5(\omega\tau,D)$	particular functions of $\omega\tau$ and D
L	effective length of RC line

LIST OF SYMBOLS (Cont'd)

M	peak amplitude of approximate base charging current
n	a constant between 1 and 2
n_c	excess electron density at the collector side of the base
n_e	excess electron density at the emitter side of the base
n_{p1}	minority carrier density at the emitter edge of the base
n_{p2}	minority carrier density at the collector edge of the base
P_{bias}	input power component delivered to bias source
$P_{d,max}$	allowable power dissipation
$P_{in,ac}$	power supplied by the drive source
$P_{in,B}$	input power delivered to the transistor
$P_{in,dc}$	collector supply power
P_L	load power
$P_{R_{BE}}$	power lost in R_{BE}
q	charge of the electron
Q_B	charge stored in the base
Q_E	bound charge in half the emitter depletion layer
R	series resistance of RC line
R_1	emitter density sampling resistance
R_2	collector density sampling resistance
R_3, C_3	differentiating network, emitter excess density
R_4, C_4	differentiating network, collector excess density
R_{BE}	portion of base resistance from the base contact to the emitter edge
R_{BI}	portion of base resistance from the edge to the center of the emitter
R_C	collector bulk resistivity

LIST OF SYMBOLS (Cont'd)

R_i	resistance approximating base current - base voltage relation
R_i'	resistance approximating the base current - base voltage relation, transistor saturated
R_L	load resistance
R_S	collector saturation resistance
S_1	storance, emitter side
S_2	storance, collector side
t	time
T	temperature in degrees Kelvin
T_C	storage time constant
v_1	emitter excess density sample voltage
v_2	collector excess density sample voltage
v_3	derivative of emitter excess density sample voltage
v_4	derivative of collector excess density sample voltage
v_B	total instantaneous base voltage
v_C	total instantaneous collector voltage
v_{CB}	voltage applied to the collector-base junction
v_{EB}	voltage applied to the emitter-base junction
v_L	load voltage
V_0	magnitude of voltage applied to RC line
$V_1(x)$	magnitude of voltage along an RC line
V_{bias}	series bias voltage used to change the apparent saturation current
V_{BB}	base bias voltage
$V_{C,min}$	minimum collector voltage

LIST OF SYMBOLS (Cont'd)

V_{CC}	collector supply voltage
$V_{CC,max}$	maximum allowable collector supply voltage
V_i	peak input signal voltage
V_{Th}	threshold base voltage (that voltage above which significant base current flows)
x	distance from driven end of RC line
X	length of linear RC line
Y	driving point admittance of RC line
Z	driving point impedance of RC line
α_i	exponent for the power function approximation of i_B
β	dc-grounded emitter current gain
γ	coefficient which approximates B by a linear function of i_C
$\theta(x)$	phase of voltage along an RC line
τ	half the time of collector current flow
τ'	half the time of saturation
ω	angular frequency
ω_α	alpha cutoff frequency

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I. INTRODUCTION

In the last few years, transistor technology has advanced rapidly with respect to the design of transistors capable of dissipating more power and operating at higher frequency. Medium power silicon mesa devices have been available since 1960 and recently experimental models of planar and epitaxial transistors with better thermal design and more sophisticated emitter geometries have been introduced. The availability of these devices has led to their investigation for use in many hf and vhf communications applications. It is expected that these transistors will soon come into widespread use. Unfortunately, very little of a theoretical nature has been written about the operation of high-efficiency, high-power transistor amplifiers at other than audio and high audio frequencies.

The object of this study has been to find ways of characterizing transistors for Class C power amplification at high and very high frequencies and to establish suitable analysis and design procedures. This will allow prediction of performance under various operating conditions, as well as optimization of the design. In addition it is hoped that the investigation will point the way toward further improvements in the devices themselves.

In Chapter II construction details of hf-vhf power transistors are presented, together with a discussion of the advantages and disadvantages of the construction for Class C power amplification.

Chapter III contains developments of three approaches suitable for analysis of low-frequency nonsaturating Class C amplifiers. The frequency of operation is considered to be low enough that the various capacitive and transit time effects are not significant factors. The internal operation of the transistor is ignored, and the problem is attacked strictly on the basis of external current-voltage characteristics. Equations are developed which relate the output power, efficiency, and power gain to the transistor parameters and the operating condition. Operating charts are developed which show the effect of choice of operating point on the output power, efficiency, and gain, allowing the designer to trade one against the other. Test results are given for 0.5-Mc and

3-Mc amplifiers which verify that, for the transistor types tested, the low-frequency analyses are quite accurate with respect to power output and efficiency. The power-gain predictions, although showing the correct trend, are more sensitive to the frequency of operation.

Chapter IV extends the simpler analytic method developed in Chapter III to the case of amplifiers which are driven into the saturation region. Equations are developed which relate the output power, efficiency, and power gain to the operating conditions and transistor parameters. The equations are necessarily rather complicated and do not lend themselves to simple maximization procedures. A numerical procedure is outlined and an example calculated for a quite practical case, that of all operating conditions constant except for the amplitude of the drive signal. The results of the computation are shown to agree well with test results.

In Chapter V, high-frequency operation is considered. The large signal high-frequency operation of the transistor is studied, based on its geometry, and the various effects that are important at high frequencies are discussed with the internal construction in mind. While it is possible to discuss the effects in some detail, the complete solution of the highly nonlinear, multidimensional problem presented is so complicated that its solution is probably not worthwhile. A number of simplifying assumptions allow a theoretical treatment to be developed which views the transistor input in a novel way as an open-end RC transmission line. In this way it is possible to obtain approximate predictions for operating in the vhf range. Test results for a 45-Mc Class C amplifier are presented which tend to verify the approach taken. Other test results are included which illustrate the various important effects occurring at high frequencies.

Chapter VI presents a new method of analog simulation of a transistor which was designed to overcome the difficulty of making a reasonably exact analysis of the internal transistor operation. A previous analog simulation, made by Beale and Beer [Ref. 1], did not include collector junction saturation. The method described in this study is based on an electrical circuit analog to the Linvill two-lump model [Ref. 2] for a portion of the base. The analogy between the Linvill two-lump model and the circuit is shown mathematically.

A schematic of the analogous circuit is presented and test results shown for a single two-lump analog. Because the analog circuitry is rather extensive, all the analogs necessary to represent transistor operation at high-frequency and large-signal levels could not be constructed. Test results are presented for a single two-lump approximation of a 5-Mc Class C amplifier.

Finally, in Chapter VII the conclusions of the study are presented, along with some suggestions of device improvements which may improve vhf power-amplifier performance.

II. HF - VHF POWER TRANSISTORS

A. VHF POWER TRANSISTOR CONSTRUCTION

Because of the requirement for high-power dissipation, vhf power transistors are primarily of silicon mesa or planar construction. This allows the collector to be mounted directly on the header and results in a small thermal resistance between the case and the collector depletion region where the heat is mainly generated.

In an attempt to reduce the collector saturation resistance to a low value and still maintain high collector breakdown voltage, vhf power transistors are generally made either by the triple-diffusion or epitaxial processes. In either case the objective is the same: to obtain a structure thick enough for easy handling and yet maintain high collector breakdown voltage, low collector saturation resistance, and low collector capacitance.

Figure 1 shows cross-section and top views of a typical transistor

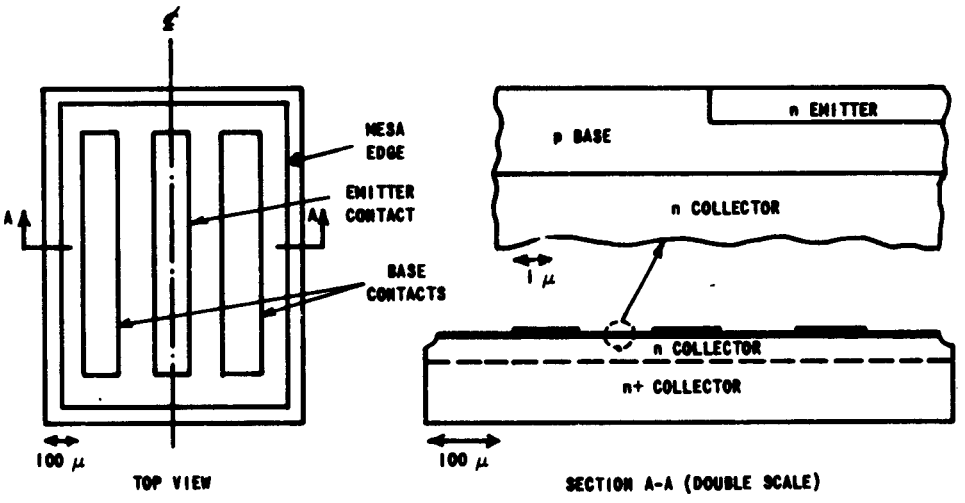


FIG. 1. TRIPLE-DIFFUSED TRANSISTOR.

of the triple-diffused type, the 2N1506. The manufacture begins with a slab of high-resistivity n-type silicon. Into one side, donor impurities are first diffused to produce the n+ collector region. A first

diffusion of acceptor impurities into the other side produces the p-type base, and a second diffusion of donor impurities through a mask on this same side produces the emitter. Because the diffusion which produces the n+ collector is quite deep and because it is first, the n collector is usually made rather wide, typically 40 to 60 microns, and the width is not too well controlled. The base and emitter diffusion depths are well controlled and produce a base width of 1.5 to 2.0 microns.

Figure 2 shows a typical doping profile for the 2N1506 transistor based on optically measured junction depths and electrically measured depletion-layer capacitances and base sheet resistance.

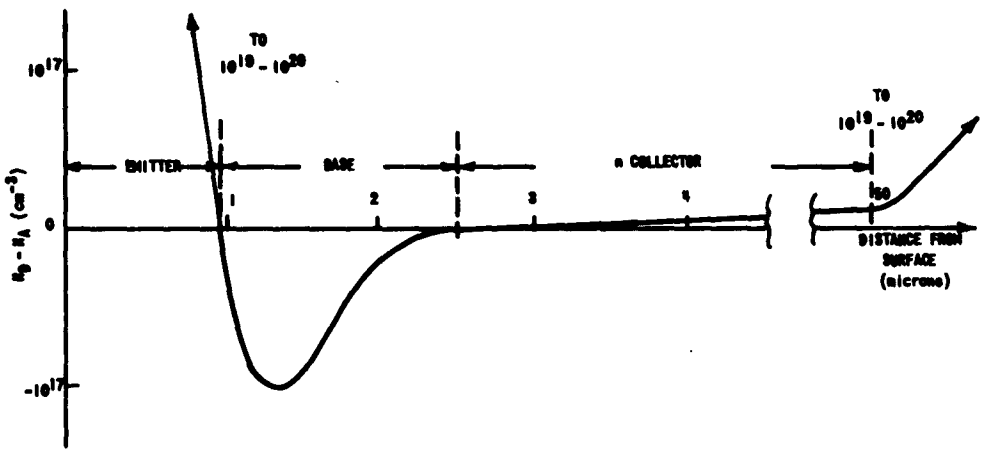


FIG. 2. IMPURITY PROFILE FOR A TRIPLE-DIFFUSED TRANSISTOR.

In the expitaxial process the manufacture begins with a low-resistivity slab of material. A high-resistivity expitaxial layer is next grown on the low-resistivity substrate. As before these form the n+ and n portions of the collector, and base and emitter diffusions are made into the n layer from the top. In this case the width of the n layer is much more easily controlled in manufacture and can therefore be made smaller. In both processes a certain amount of diffusion occurs at the n:n+ interface so that the doping does not change abruptly there. An additional refinement is the surface passivation process where the

surface is protected by a silicon oxide coating after the epitaxial growth step. The base and emitter diffusions are performed through windows opened in the coating by photoresist techniques; and since diffusion proceeds laterally as well as vertically, the resulting junction edges are formed under the oxide coating. This reduces surface recombination, increasing β particularly at low collector currents.

At high frequencies and high current levels the emitter current flows into the base mainly at the edge of the emitter. For this reason, emitter geometries with a large ratio of perimeter to area are common. The stripe geometry is shown in Fig. 1; while Fig. 3 shows the star geometry of the of the MM487, and Fig. 4 the interdigitated structure of the TA2084 and the SN102 transistors. The interdigitated structure is seen to achieve a very high perimeter-to-area ratio.

B. FAVORABLE AND UNFAVORABLE ASPECTS OF PRESENT VHF POWER TRANSISTORS

The vhf power transistors in present use achieve good power dissipation. They have relatively low collector capacitance and high collector breakdown voltage. Power gain is high at low frequencies and does not drop to unity until the frequency of operation rises to 150 to 250 Mc.

On the other hand, a number of unfavorable aspects remain. Some of them are:

1. Power-dissipation ratings available do not yet compare to vacuum tubes.
2. The frequency is limited at the upper end by the fact that as the base is made thinner, the resulting high sheet resistivity does not allow the input signal to penetrate to the interior of the transistor.
3. The collector-base junction is from two to four times the area of the emitter-base junction. Most of the portion of the collector junction which is not opposite the emitter junction serves no useful purpose. Instead, the capacitance of that portion provides a feedback path to the base which may require neutralization.
4. Electrical connection of the collector to the case complicates circuit design. To maintain the case temperature as close to ambient as possible, the transistor should be mounted directly on a metal chassis which acts as a heat sink and ground reference. If this is done, both emitter and base circuits must be isolated from ground. A second approach is to place a beryllium oxide wafer between the transistor case and the metal chassis. BeO has

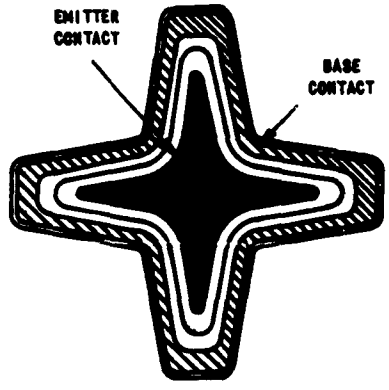


FIG. 3. STAR TRANSISTOR GEOMETRY.

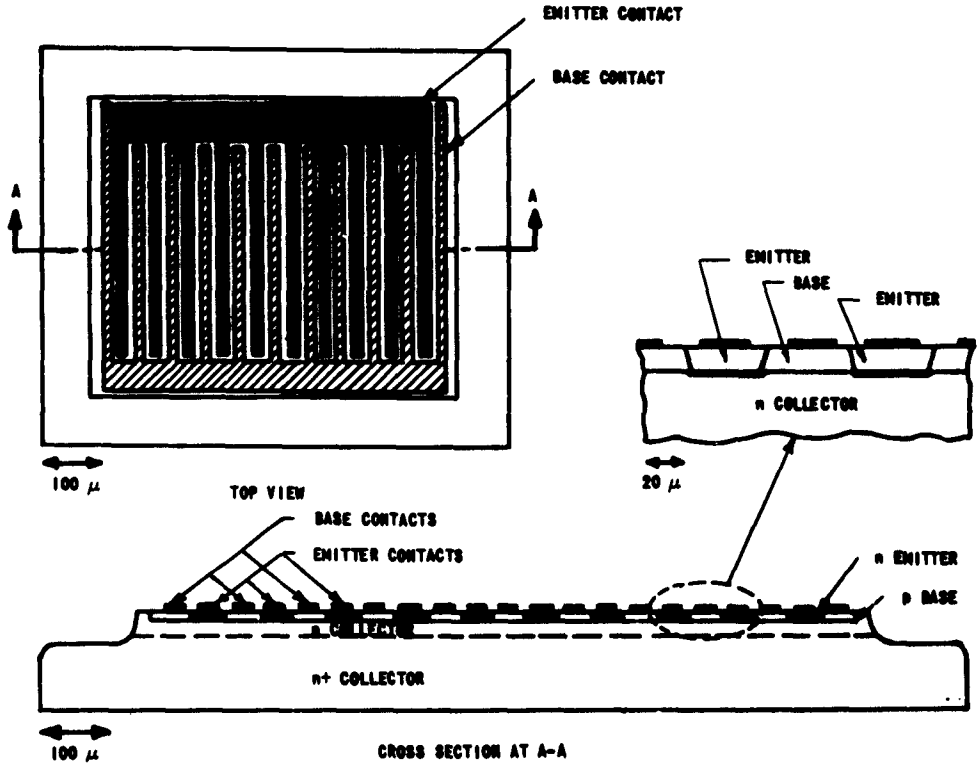


FIG. 4. INTERDIGITATED TRANSISTOR GEOMETRY.

thermal conductivity midway between aluminum and copper but is an excellent insulator. This allows the emitter to be connected to the chassis but does add several picofarads of additional output capacitance. It is suggested for future designs that the semiconductor wafer be mounted on a BeO wafer inside the case and that the emitter be connected to the case internally. This would reduce the degenerative emitter lead inductance to a minimum, while the collector-to-ground capacitance added in this manner would be much less than if the entire case were insulated.

5. Because the high-resistivity portion of the collector does not occur entirely within the collector depletion region, the advantages of a low-resistivity substrate in producing low saturation resistance are presently not being realized fully. Collector current emerges from the depletion region in a very dense distribution under the emitter edge. As the current flows toward the n+ region, it spreads out and produces less voltage drop. Since the major portion of the voltage drop occurs in the initial spreading phase, it would be valuable to make the n layer quite thin and with a very high resistivity so that even at quite low collector voltage the collector current would emerge into the low-resistivity substrate.

Although present vhf transistors are quite advanced devices, it is expected that both the upper frequency and power capability will be further improved in the next few years and that their usage in hf and vhf transmitters will increase.

III. LOW FREQUENCY NONSATURATING CLASS C AMPLIFIERS

A. INTRODUCTION

Class C amplifiers are used primarily to achieve high output power at high efficiency. The power gain is often an important consideration also. As emitter-base bias conditions are changed to obtain higher efficiency, the power gain generally decreases. Therefore, analysis and design procedures which clearly show the effect of variation of operating conditions are valuable. In this chapter, three methods of analysis will be developed which are suitable for low-frequency, non-saturating Class C amplifiers. Limitations on the operating conditions are defined by the transistor current, voltage, and power ratings. The effect of these limitations is also conveniently shown.

Transistorized Class C amplifiers operate basically in the same way as vacuum-tube Class C amplifiers. Figure 5 shows a simplified circuit

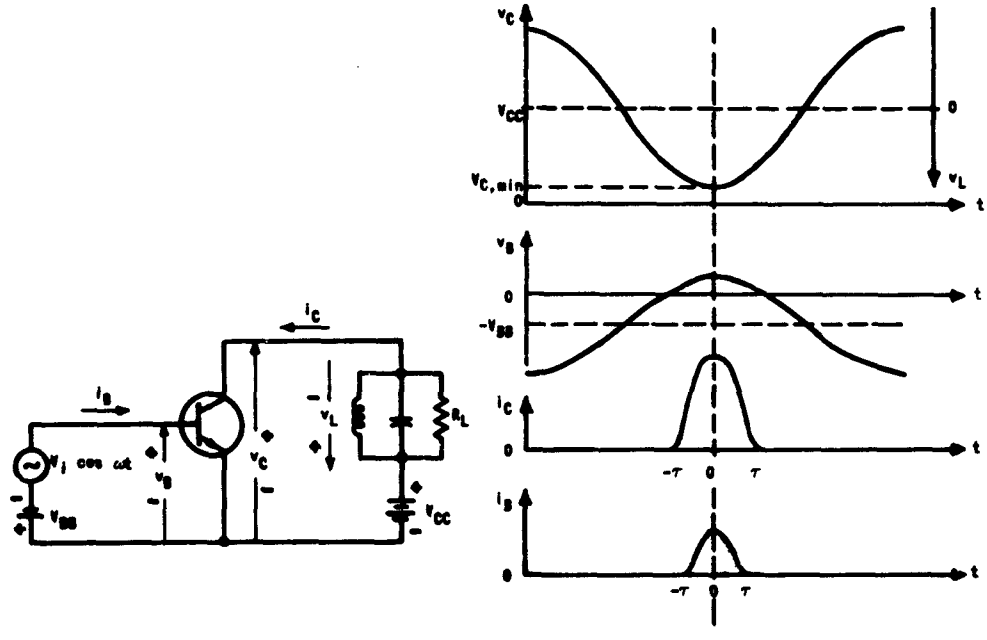


FIG. 5. BASIC CLASS C OPERATION.

diagram and waveforms illustrating typical operation. The tuned circuits used in both the input and output have high enough Q so that the collector and base voltages may be considered sinusoidal. A loaded Q of 10 or greater is common although in some cases it may unavoidably be as low as 5. This report will be limited to consideration of those cases where the transistor voltages may be approximated by sinusoids.

The collector and base currents flow primarily in response to the base voltage, and flow in pulses of less than 180 deg width at the time the base voltage is positive. The collector-current pulses excite the load circuit which, if tuned to the frequency of the drive, responds with a nearly sinusoidal voltage 180 deg out of phase with the input. Because the collector current flows at a time when v_C is small and v_L is large, the energy delivered to the load circuit is large while the energy dissipated by the transistor is small. In these respects the principles of operation of transistor amplifiers are the same as for vacuum-tube amplifiers. Many differences will be seen in Chapter V where high-frequency operation is considered. Some differences which are important at low frequencies are:

1. Transistors are low-voltage high-current devices. Typical vhf power transistors have a maximum peak collector-current rating of 0.5 to 5 amp and a maximum collector-voltage rating of 60 to 150 v. The reverse-biased emitter-base breakdown voltage may be 5 to 10 v.
2. In a transistor amplifier, input current flows during the entire time of output-current flow; whereas in a vacuum-tube amplifier, grid current flows only when the grid is driven positive.
3. A zero-biased silicon transistor ($V_{BB} = 0$) operated from a low-impedance source results naturally in Class C operation. This is so because significant collector current does not flow until the emitter-base junction has been forward biased by 0.6 to 0.7 v.
4. The device temperature is an important factor in the current-voltage characteristics in the case of a transistor. To take account of this factor the static transistor characteristics may be taken by pulse measurement in a high ambient temperature environment. In this way the device temperature can be set near that expected in operation and the amount of heating caused by the measurement made negligible. A pulse width of a few microseconds is usually sufficient to establish steady-state conditions and is much shorter than the thermal time constant of the transistor.

In this chapter the frequency of operation will be considered to be low enough that the various capacitive and transit time effects are not significant factors. This is an appropriate assumption for many vhf power transistors in the frequency range up to a few megacycles, and it allows a development which most clearly illustrates the effects of choice of operating condition on power output, power gain, and efficiency.

Also, the transistor is assumed to operate only in the cutoff and active regions. Neglecting the possibility of operation into collector saturation greatly simplifies the analysis. It is found that nonsaturating low-frequency amplifiers, because of low saturation resistance, have high efficiency and high output power and are therefore of interest. The results obtained also form a boundary for the saturating case and point out the trends for operation in saturation.

The analytical approach which will be used in this chapter will be to ignore the internal workings of the transistor and to attack the problem strictly on the basis of external current-voltage characteristics. The problem then becomes one of how to work with these nonlinear, large-signal characteristics either graphically or analytically. The graphical method given is a direct carry-over from Class C vacuum-tube design. The two analytic methods approximate the characteristics with simple functions which may be handled mathematically. The second and more exact approximation in particular appears to be a new treatment.

B. ANALYSIS OF A SIMPLE LARGE-SIGNAL TRANSISTOR MODEL

Figure 6 shows the dc collector characteristics and the emitter-base characteristics for a typical vhf power transistor. The emitter-base characteristics are nearly independent of the collector voltage as long as the collector voltage is large enough not to be in the saturation region. The dashed line shown in Fig. 6a indicates the approximate beginning of saturation.

The approximations to be made in this model are indicated in Fig. 7. The input is approximated by a biased ideal diode and a linear resistance. The values of V_{Th} and R_i are determined by the range of operation one wishes to consider. In the example shown, the range of expected peak collector current is 0.1 to 0.8 amp and the corresponding base

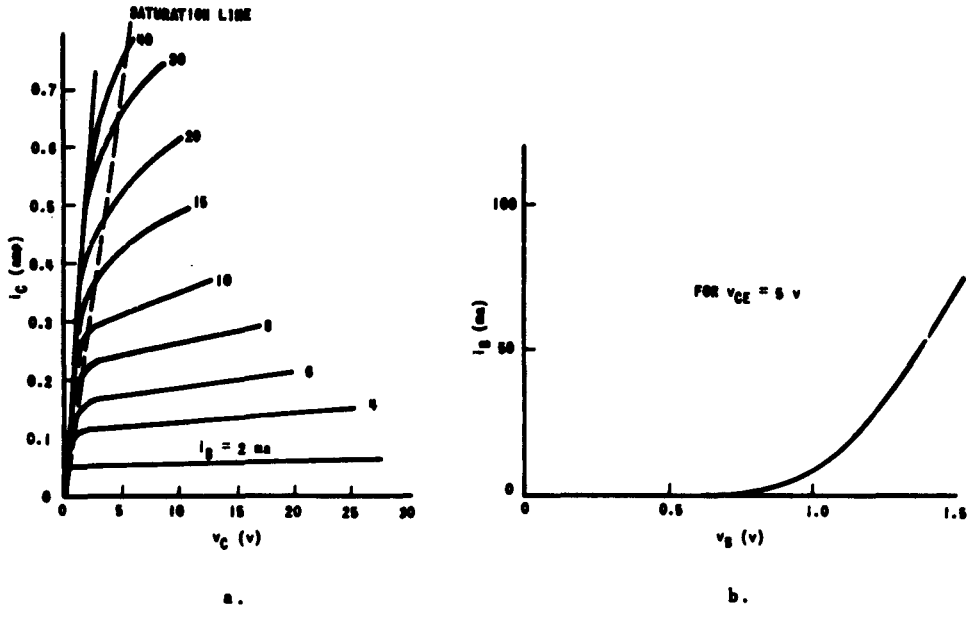


FIG. 6. TYPICAL CHARACTERISTICS, COMMON EMITTER.

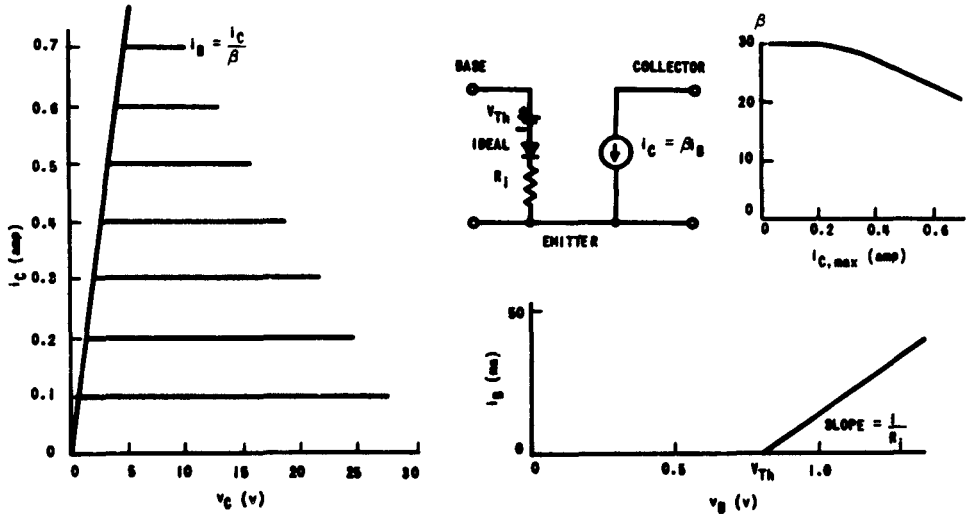


FIG. 7. APPROXIMATE CHARACTERISTICS, COMMON EMITTER.

current range of greatest interest is 4 to 40 ma. V_{Th} and R_i were obtained by inspection of the best fit of i_B up to 40 ma. The collector current is approximated by a constant (β) times the base current. In this model β is a function of $I_{C,max}$ and is determined along the dashed saturation line shown in Fig. 6a. Figure 7 also shows β vs $I_{C,max}$ determined in the same way.

When this model is used in the circuit of Fig. 5, the base and collector currents are sections of sine waves as follows:

$$i_B = \frac{I_{B,max}}{1 - \cos \omega\tau} [\cos \omega t - \cos \omega\tau] \qquad (1)$$

$$i_C = \frac{I_{C,max}}{1 - \cos \omega\tau} [\cos \omega t - \cos \omega\tau] \qquad (2)$$

for $-\tau < t < \tau$ and $i_B = 0 = i_C$ during the rest of the cycle. τ is defined as half the time of current flow.

The input ac power is

$$P_{in,ac} = \frac{\omega}{2\pi} \int_{-\pi/\omega}^{\pi/\omega} V_i \cos \omega t \; i_B \, dt \qquad (3)$$

It will be convenient to have the final result in terms of $I_{C,max}$, the peak collector current, and $\omega\tau$, the half angle of current flow. To relate V_i to $I_{C,max}$ note that the peak base current occurs at $t = 0$ when

$$I_{B,max} = \frac{V_i - (V_{BB} + V_{Th})}{R_i}$$

The currents become zero at $t = \pm\tau$ when

$$V_i \cos \omega\tau = V_{BB} + V_{Th}$$

Combining these and noting that $I_{C,max} = \beta I_{B,max}$ gives

$$V_i = \frac{R_i}{\beta(1 - \cos \omega\tau)} I_{C,max} \tag{4}$$

Substituting (1) and (4) in (3) and performing the integration gives

$$P_{in,ac} = \frac{R_i I_{C,max}^2}{\pi\beta^2(1 - \cos \omega\tau)^2}\left[\frac{\omega\tau}{2} + \frac{\sin 2\omega\tau}{4} - \cos \omega\tau \sin \omega\tau\right] \tag{5}$$

Next consider the output circuit. The input dc power is

$$P_{in,dc} = \frac{\omega}{2\pi} \int_{-\pi/\omega}^{\pi/\omega} V_{CC} i_C dt \tag{6}$$

Substituting (2) and integrating gives

$$P_{in,dc} = \frac{V_{CC} I_{C,max}}{\pi(1 - \cos \omega\tau)} [\sin \omega\tau - \omega\tau \cos \omega\tau] \tag{7}$$

The power delivered to the load is

$$P_L = \frac{\omega}{2\pi} \int_{-\pi/\omega}^{\pi/\omega} v_L \, i_C \, dt \tag{8}$$

Noting that

$$v_L = (V_{CC} - V_{C,min}) \cos \omega t \tag{9}$$

and substituting (2) and (9) and integrating gives

$$P_L = \frac{I_{C,max}(V_{CC} - V_{C,min})}{\pi(1 - \cos \omega\tau)} \left(\frac{\omega\tau}{2} + \frac{\sin 2\omega\tau}{4} - \cos \omega\tau \sin \omega\tau\right) \tag{10}$$

The collector efficiency is

$$E_c \triangleq \frac{P_L}{P_{in,dc}} = \frac{V_{CC} - V_{C,min}}{V_{CC}} \left(\frac{\frac{\omega\tau}{2} + \frac{\sin 2\omega\tau}{4} - \cos \omega\tau \sin \omega\tau}{\sin \omega\tau - \omega\tau \cos \omega\tau} \right) \qquad (11)$$

The power gain is

$$G \triangleq \frac{P_L}{P_{in,ac}} = \frac{\beta^2 (V_{CC} - V_{C,min})(1 - \cos \omega\tau)}{I_{C,max} R_i} \qquad (12)$$

Equations (10), (11), and (12) are the results of the analysis. They show how output power, efficiency, and power gain are related to the operating conditions for any operating condition out of saturation. A further restriction is natural and illuminating, however. It is obvious from (11) that for maximum efficiency $V_{C,min}$ should be as small as possible. The limit in this direction for this analysis is the collector saturation voltage. Suppose, then, that $V_{C,min} = R_S I_{C,max}$. The equations then become

$$\left.\begin{aligned} P_L &= I_{C,max}(V_{CC} - R_S I_{C,max})\, K_1(\omega\tau) \\ E_C &= \frac{(V_{CC} - R_S I_{C,max})}{V_{CC}} \frac{K_1(\omega\tau)}{K_2(\omega\tau)} \\ G &= \frac{\beta^2 (V_{CC} - R_S I_{C,max})}{I_{C,max} R_i} (1 - \cos \omega\tau) \end{aligned}\right\} \qquad (13)$$

where

$$K_1(\omega\tau) = \frac{\frac{\omega\tau}{2} + \frac{\sin 2\omega\tau}{4} - \cos \omega\tau \sin \omega\tau}{\pi(1 - \cos \omega\tau)}$$

$$K_2(\omega\tau) = \frac{\sin \omega\tau - \omega\tau \cos \omega\tau}{\pi(1 - \cos \omega\tau)}$$

With subsidiary design equations,

$$\left.\begin{aligned} R_L &= \frac{1}{2}\frac{(V_{CC} - R_S I_{C,max})^2}{P_L} \\ V_i &= \frac{R_i}{\beta(1 - \cos \omega\tau)} I_{C,max} \\ V_{BB} &= \frac{R_i}{\beta(1 - \cos \omega\tau)} I_{C,max} \cos \omega\tau - V_{Th} \end{aligned}\right\} \quad (13a)$$

The set of Eqs. (13) and (13a) shows the result of operating with a certain V_{CC}, with bias and drive such as to give a certain $\omega\tau$ and $I_{C,max}$ and with a load resistance such as to cause the collector voltage to drop just to saturation at the extreme of the cycle. Often V_{CC} is specified to the designer. If it is not, it should be made as large as possible within the breakdown voltage capability of the transistor as this maximizes P_L, E_C, and G. The design then becomes a question of choosing $\omega\tau$ and $I_{C,max}$. It is convenient to plot P_L, E_C, and G on $I_{C,max}$ - $\omega\tau$ coordinates. Table 1 gives values of $K_1(\omega\tau)$, $K_2(\omega\tau)$, K_1/K_2, and $(1 - \cos \omega\tau)$ which make the construction of the plot easy.

TABLE 1. VALUES OF FLOW-ANGLE CONSTANTS

$\omega\tau$ (deg)	K_1	K_2	K_1/K_2	$1 - \cos \omega\tau$
90	0.250	0.318	0.787	1.000
80	.236	.286	.825	0.827
70	.217	.253	.859	.658
60	.195	.218	.894	.500
50	.170	.182	.928	.357
40	.139	.148	.933	.234
30	.105	.112	.937	.134

Figure 8 is an example of a plot using the data of Figs. 6 and 7 for the 2N1506 (V_{CC} = 40 v), with V_{Th} = 0.8, R_S = 7Ω, R_i = 14Ω, and β

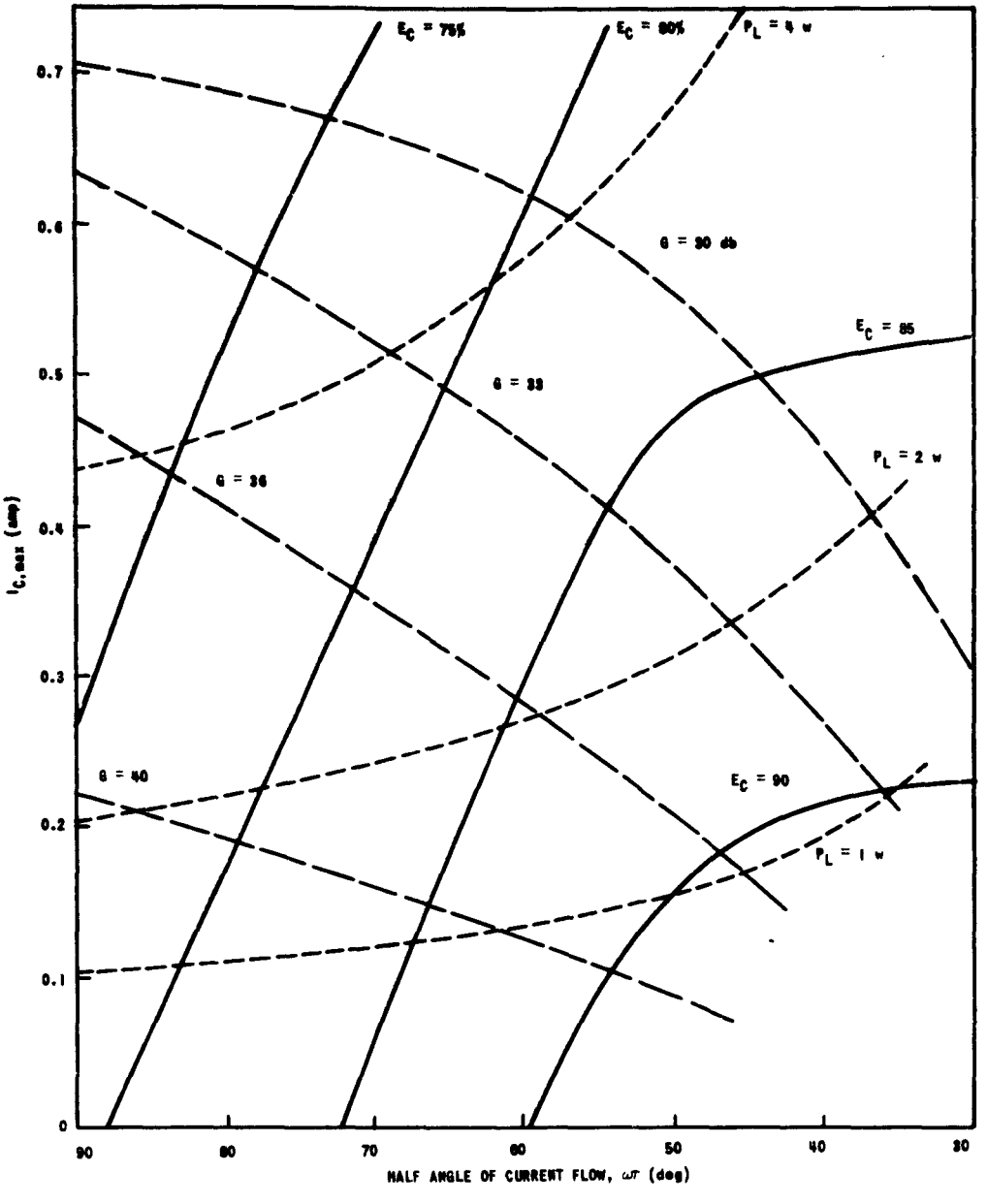


FIG. 8. OPERATING CHART FOR THE 2N1506 TRANSISTOR, FIRST ANALYSIS (V_{CC} = 40 v).

as given in Fig. 7. It takes about 2 hr to construct such a plot. Once it is available, however, it shows a wide range of possible operation. Suppose a 2-w output were desired. Figure 8 shows that a maximum efficiency of 87 percent is possible but that the power gain will be 6 db less than when operating Class B with 76 percent efficiency. In general, Fig. 8 shows that a given output power can be obtained at higher efficiency by operating with larger peak current and smaller angle of flow, but that in so doing the power gain is less.

C. A GRAPHICAL ANALYSIS

The model analyzed in the preceding section is simple enough that the derivation and use of the applicable design equations is straightforward. As is obvious by comparison of Figs. 6 and 7, however, the approximation of the transistor characteristics is not very accurate. In this and the following section, more accurate methods are developed.

A graphical analysis which has long been used for vacuum-tube Class C amplifiers makes use of the fact that the plate and grid voltages are both sinusoidal and 180 deg out of phase. When the tube characteristics are taken and plotted on plate voltage - grid voltage coordinates, the operating path becomes a straight line. This method is directly applicable to transistor Class C amplifiers. Figure 9 is a set of collector and base characteristics for the 2N1506 plotted on collector voltage - base voltage coordinates. The operating line for assumed bias, drive, and load conditions is shown. A point on this line relates instantaneous values of base voltage, collector voltage, base current, and collector current. For any assumed bias point and maximum operating point, the waveforms of all currents and voltages are determined by the motion of the instantaneous operating point along the operating line. The voltages may be constructed sinusoidally about the bias voltages, and the currents constructed by projecting from the instantaneous operating point to the voltage waveform and thence to the current value. A typical projection for a collector current of 0.4 amp is shown.

Once all of the currents and voltages have been obtained, the value of $P_{in,ac}$ can be obtained by integrating, $P_{in,ac} = \int i_B V_i \cos \omega t dt$.

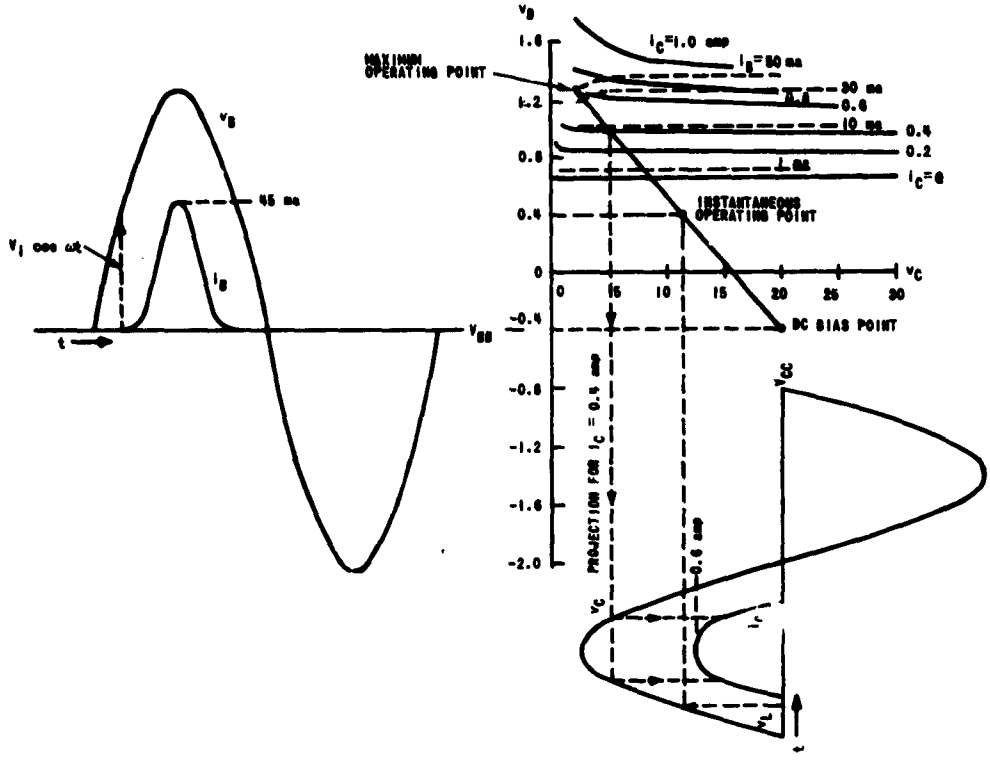


FIG. 9. CONSTANT CURRENT CHARACTERISTICS FOR THE 2N1506 TRANSISTOR.

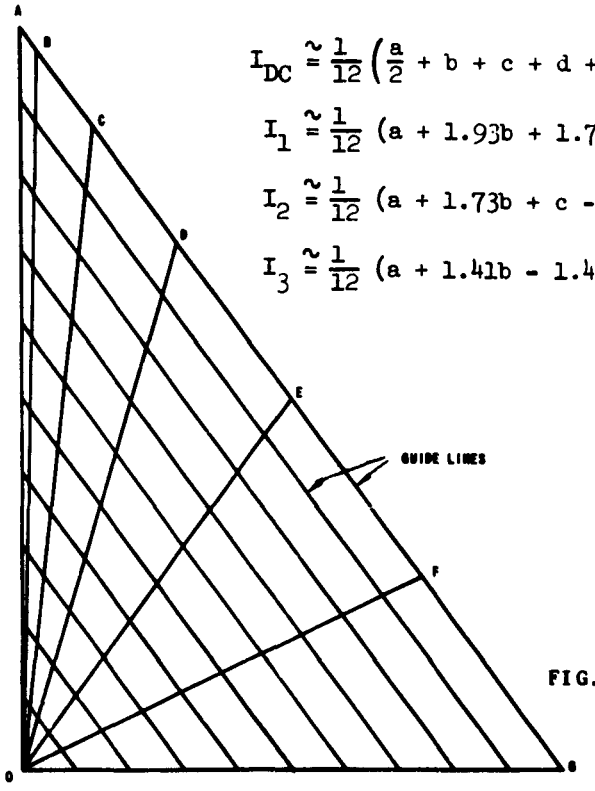
Likewise $P_{in,dc} = V_{CC}\int i_C dt$ and $P_L = \int v_L i_C dt$ can be obtained by graphical integration. Efficiency and power gain can be obtained from these powers. This procedure is simplified by the use of the graphical performance computor shown in Fig. 10 [Ref. 3]. This computer is essentially a way of approximately obtaining the zero frequency (I_{DC}), fundamental frequency (I_1), and harmonic (I_2, I_3) components of the current pulses. When these are known,

$$
\begin{aligned}
P_{in,dc} &= I_{CDC}\, V_{CC} \\
P_{bias} &= I_{BDC}\, V_{BB} \\
P_{in,ac} &= \tfrac{1}{2}\, I_{B1}\, V_i \\
P_L &= \tfrac{1}{2}\, I_{C1}\, (V_{CC} - V_{C,min})
\end{aligned}
\qquad (14)
$$

Note that P_{bias} represents power delivered to the bias battery when V_{BB} is positive (usual Class C bias). The portion of the input power actually delivered to the base is

$$P_{inB} = P_{in,ac} - P_{bias} \qquad (15)$$

The computer of Fig. 10 is reproduced on transparent plastic and is



$$
\left.
\begin{aligned}
I_{DC} &\approx \frac{1}{12}\left(\frac{a}{2} + b + c + d + e + f\right) \\
I_1 &\approx \frac{1}{12}\,(a + 1.93b + 1.73c + 1.41d + e + 0.52f) \\
I_2 &\approx \frac{1}{12}\,(a + 1.73b + c - e - 1.73f) \\
I_3 &\approx \frac{1}{12}\,(a + 1.41b - 1.41d - 2e - 1.41f)
\end{aligned}
\right\} \qquad (16)
$$

FIG. 10. PERFORMANCE COMPUTER [Ref. 3].

used in the following way. On a set of constant current transistor characteristics draw an operating line from the assumed dc bias point to the assumed maximum operating point. Lay the computer over the characteristics with the guide lines parallel to the operating line. Keeping these parallel, adjust the computer until the dc bias point falls on OG and the maximum operating point falls on OA. Read the currents where the lines OA, OB, etc., intersect the operating line. These values are a, b, etc., which may be used in Eqs. (16) in Fig. 10 to obtain the various components of current. The use of Eqs. (14) then completes the analysis.

The advantages of this method are:

1. The actual characteristics are used and for this reason the results are more accurate.
2. The method applies also to operation into saturation if the frequency is sufficiently low. (For reasons to be seen later, saturation lowers the frequency limit for which static methods are applicable.)

The disadvantages of this method are:

1. The use of a finite number of points to Fourier analyze the current pulses is an approximation.
2. The method analyzes only one situation. In order to optimize, or even to design for a specific condition such as a given output power, one must analyze one set of end-points, then analyze another and see if the operation is more satisfactory. This is rather time consuming and not very informative.

D. A MORE ACCURATE ANALYTIC METHOD

1. Development of the Model

The method presented in Sec. B had the drawback that the model only approximated the transistor in a crude way. It would be desirable to have a model which was more accurate but which still was simple enough to be handled analytically in an exact way. To achieve these ends let us consider first the output circuit.

The constant current characteristics for the 2N1506 are given in Fig. 11. Over a large portion of the range these characteristics are practically straight lines. Where they begin to curve appreciably

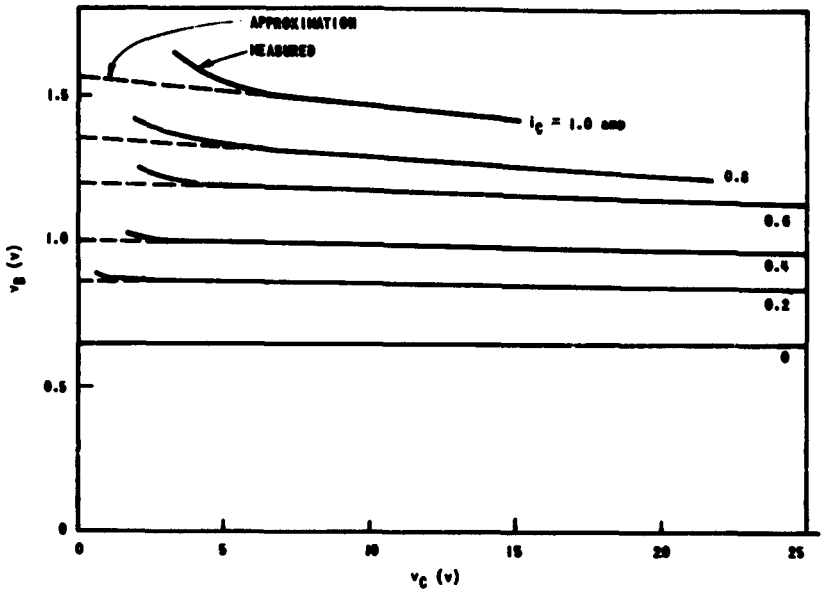


FIG. 11. CONSTANT CURRENT CHARACTERISTICS.

the transistor is in the saturation region. Since we are not considering operation in saturation here, let us approximate the actual characteristics by straight lines (shown dashed in Fig. 11). Then for any i_C, v_B is a linear function of v_C,

$$v_B = A + B\, v_C \tag{17}$$

where A and B are functions of i_C. Evidently A is the value of v_B when $v_C = 0$, i.e., the intercepts of the constant i_C lines with the vertical axis. Also, since A is a function of i_C only,

$$B = \frac{\partial v_B}{\partial v_C} \tag{18}$$

That is, B is the slope of the constant i_C lines. If simple functions can be found for A and B in terms of i_C, then a simple relationship can be established between i_C, v_B, and v_C.

Figure 12 is a plot of A vs i_C. Evidently A is well approximated by a linear function of i_C.

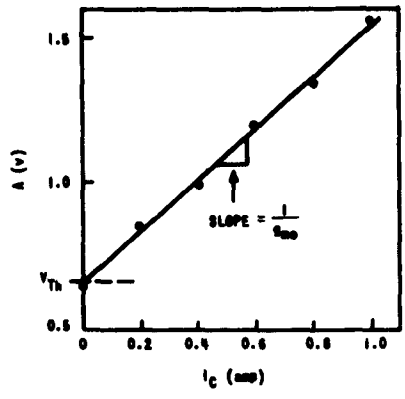


FIG. 12. APPROXIMATION FOR A.

$$A = V_{Th} + \frac{1}{g_{mo}} i_C \tag{19}$$

where V_{Th} is the value of A when $i_C = 0$ for the best straight-line fit to the plotted points and $1/g_{mo}$ is the slope of that line. V_{Th} is the threshold base voltage, i.e., that voltage above which collector current flows; and g_{mo} is the zero collector-voltage transconductance, i.e.,

$$g_{mo} = \frac{\partial i_C}{\partial v_B}\bigg|_{v_C=0} \tag{20}$$

Figure 13 is a plot of B vs i_C. This has been approximated by a linear function

$$B = \gamma i_C \tag{21}$$

A power approximation would evidently be much better; however, this term has a minor effect on i_C and the linear equation will be used because of the difficulty of handling a power approximation in later work.

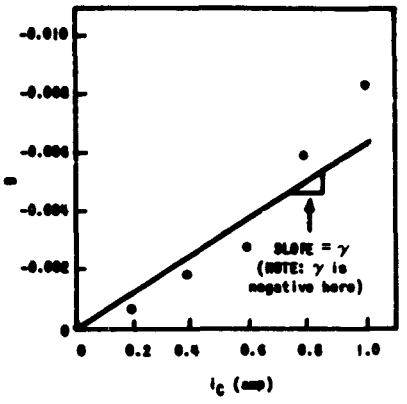


FIG. 13. APPROXIMATION FOR B.

Substituting (19) and (21) in (17) and solving for i_C gives the final result

$$i_C = \frac{v_B - V_{Th}}{\frac{1}{g_{mo}} + \gamma v_C} \tag{22}$$

At this point two questions may come to mind:

1. Does this procedure lead to as satisfying an approximation for other vhf transistors?
2. After the many approximations made here, how well does Eq. (22) represent the collector-current pulse for various v_C and v_B conditions?

Without presenting the complete procedure, let us refer to Fig. 14 which shows A and B for an MM487 (star) transistor, and Fig. 15 which shows A and B for the TA2084. Evidently the procedure works generally well for approximating A and generally poorly for approximating B.

Regarding the second question, Fig. 16 shows comparative collector-current waveforms for the three methods of analysis under the same collector- and base-voltage conditions. The graphical method gives the exact result. It is apparent that the use of Eq. (22) gives significantly better results than the first analytic method, and in fact gives results that are quite close to the exact waveform. Similar results were obtained when applying this test to the other transistors.

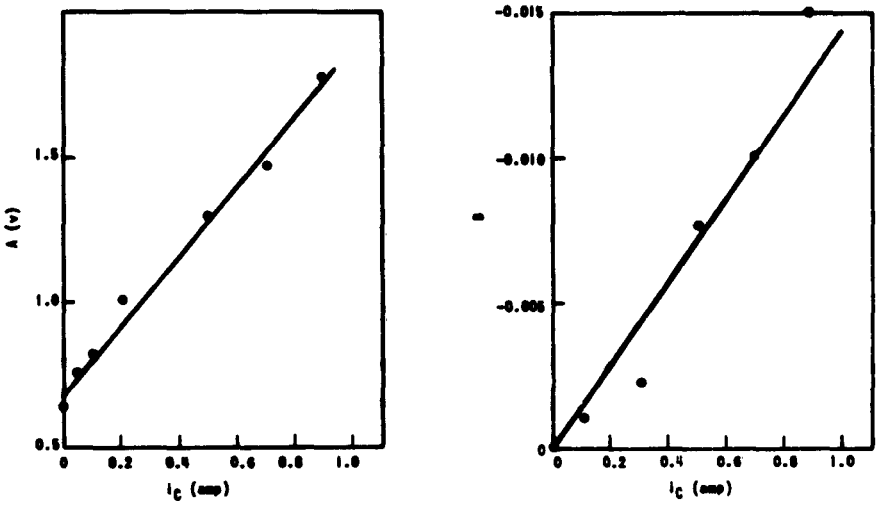


FIG. 14. APPROXIMATIONS FOR THE MM487 TRANSISTOR.

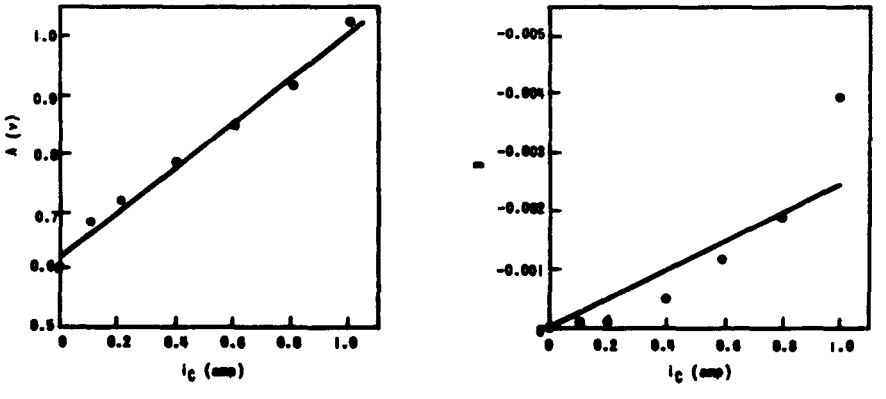


FIG. 15. APPROXIMATIONS FOR THE TA2084 TRANSISTOR.

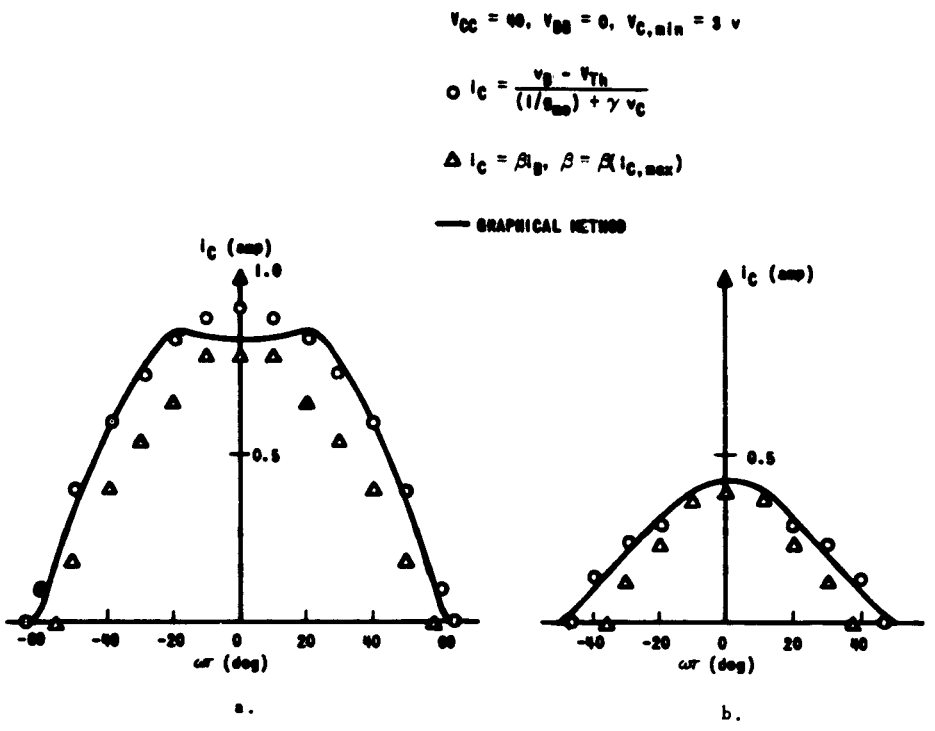


FIG. 16. COLLECTOR-CURRENT WAVEFORMS FOR THE 2N1506 TRANSISTOR.

After a number of trials it was discovered that a surprisingly accurate approximation for the input circuit could be obtained over the range of base currents of interest (1 to 100 ma) by

$$\left.\begin{aligned} i_B &= G_i(v_B - V_{Th})^{\alpha_i}, \quad v_B \geq V_{Th} \\ i_B &= 0, \quad v_B < V_{Th} \end{aligned}\right\} \tag{23}$$

Figure 17 is a plot of i_B vs $v_B - V_{Th}$ on logarithmic scales for the three types of transistor studied. It is evident that this approximation is excellent over the entire range of appropriate base currents for all three transistor types.

The complete model is shown schematically in a Class C amplifier circuit in Fig. 18.

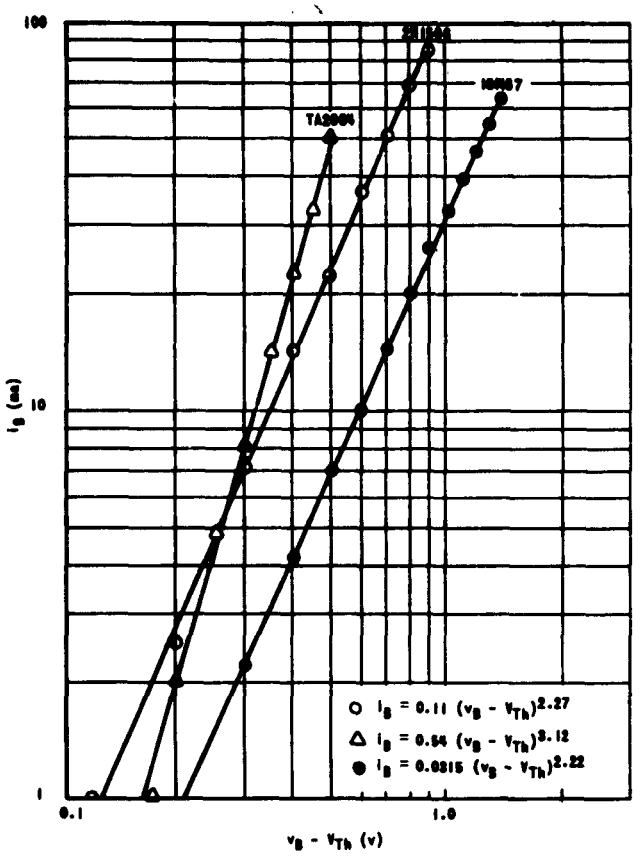


FIG. 17. INPUT CHARACTERISTICS.

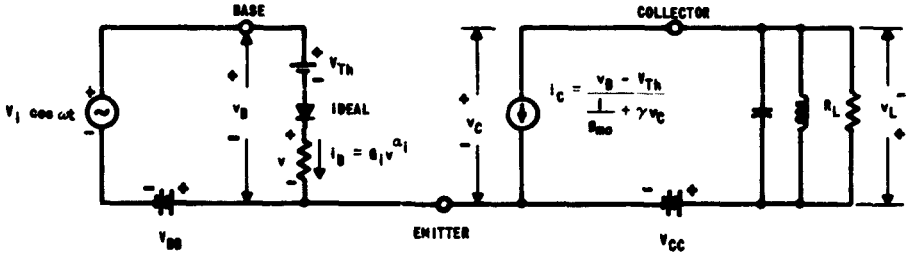


FIG. 18. ACCURATE MODEL IN CLASS C AMPLIFIER.

2. Analysis of a Class C Amplifier Using the Model

The same assumptions as before are now made concerning the voltages. That is, since we are considering low-frequency, nonsaturating operation with high Q tuned circuits in both input and output, the base and collector voltages are sinusoidal and 180 deg out of phase.

From Eq. (3) the input ac power is

$$P_{in,ac} = \frac{\omega}{2\pi}\int_{-\pi/\omega}^{\pi/\omega} V_i \cos \omega t \; i_B dt$$

In this case the base current is

$$i_B = G_i \left(V_i \cos \omega t - V_{BB} - V_{Th}\right)^{\alpha_i}, \qquad \tau < t < \tau \tag{24}$$

Using also

$$\cos \omega\tau = \frac{V_{BB} + V_{Th}}{V_i} \tag{25}$$

Eq. (3) now becomes

$$P_{in,ac} = \frac{G_i V_i^{(1 + \alpha_i)}}{\pi} K_3(\omega\tau, \alpha_i) \tag{26}$$

where

$$K_3(\omega\tau, \alpha_i) = \int_0^{\omega\tau} \cos \omega t [\cos \omega t - \cos \omega\tau]^{\alpha_i} d(\omega t) \tag{27}$$

This can be integrated in terms of simple functions for α_i an integer. However, it appears from Fig. 17 that α_i will rarely be an integer. Equation (27) can be evaluated numerically, of course, for any α_i. This has been done by a computer and the results are plotted in Fig. 19. For any transistor whose constants, V_{Th}, G_i, and α_i are known, the use of Eqs. (25) and (26) and Fig. 19 will yield the input ac power.

Before beginning the development of the equations for the output circuits, it will be convenient to express the collector current pulse in a form which is more informative and which is more easily handled

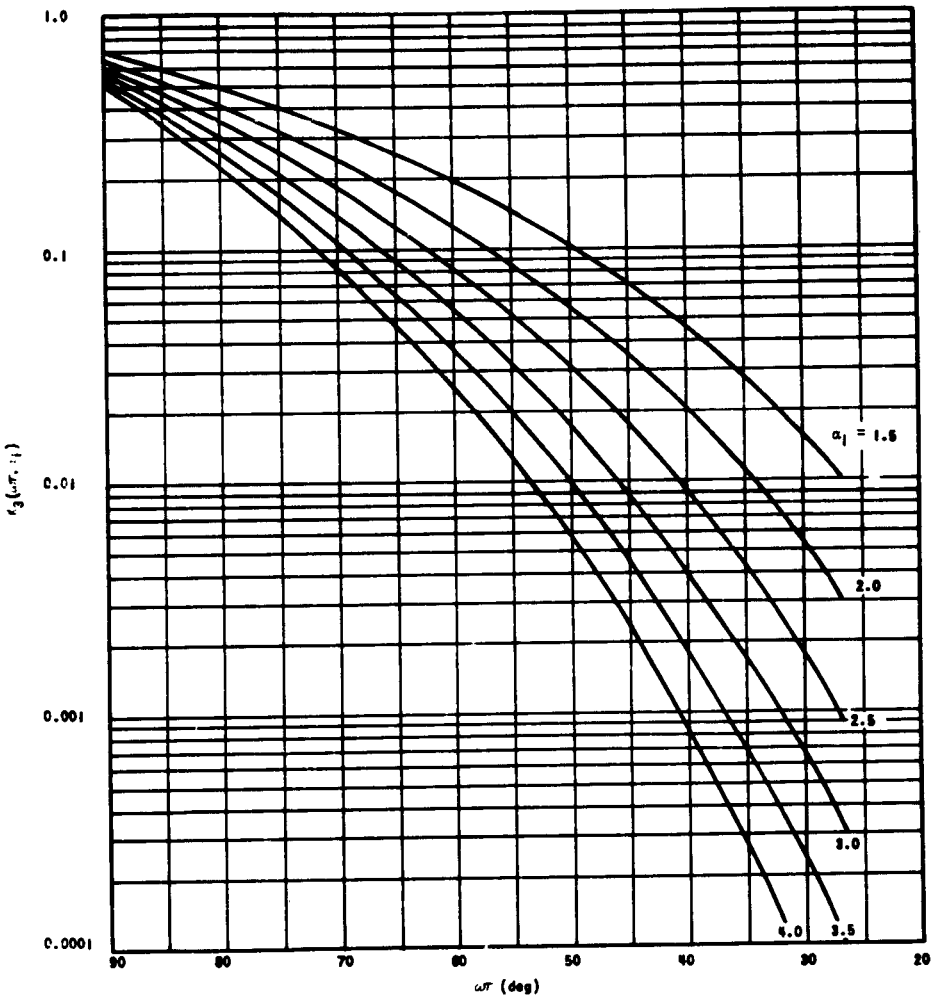


FIG. 19. VALUES OF K_3.

in the integrals. In the Class C circuit the base and collector voltages are

$$v_B = V_i \cos \omega t - V_{BB} \tag{28}$$

$$v_C = V_{CC} - (V_{CC} - V_{C,min}) \cos \omega t \tag{29}$$

When these are substituted in Eq. (22) the collector current becomes

$$i_C = \frac{V_i \cos \omega t - V_{BB} - V_{Th}}{\frac{1}{g_{mo}} + \gamma \left[V_{CC} - (V_{CC} - V_{C,min}) \cos \omega t\right]} \tag{30}$$

$$i_C = V_i \frac{\cos \omega t - \frac{V_{BB} + V_{Th}}{V_i}}{\frac{1}{g_{mo}} + \gamma V_{CC} - \gamma (V_{CC} - V_{C,min}) \cos \omega t} \tag{31}$$

$$i_C = V_i \frac{\cos \omega t - \cos \omega \tau}{\frac{1}{g_{mo}} + \gamma V_{CC} - \gamma (V_{CC} - V_{C,min}) \cos \omega t} \tag{32}$$

Setting $t = 0$ in the last equation gives the maximum current

$$I_{C,max} = V_i \frac{1 - \cos \omega \tau}{\frac{1}{g_{mo}} + \gamma V_{C,min}} \tag{33}$$

which we solve for V_i and insert in Eq. (32). After some more algebraic manipulation this is finally written as

$$I_C = I_{C,max} \left[\frac{1 - D}{1 - \cos \omega \tau} \frac{\cos \omega \tau - \cos \omega t}{D - \cos \omega \tau}\right] \tag{34}$$

where

$$D \triangleq \frac{\frac{1}{\gamma g_{mo}} + V_{CC}}{V_{CC} - V_{C,min}} \tag{35}$$

In this form the dc component of collector current is found by integration to be

$$\frac{I_{CDC}}{I_{C,max}} \triangleq K_4(\omega\tau, D)$$

$$= \begin{cases} \dfrac{1 - D}{\pi(1 - \cos \omega\tau)} \left[\omega\tau - \dfrac{D - \cos \omega\tau}{\sqrt{D^2 - 1}} \tan^{-1}\left(\dfrac{\sqrt{D^2 - 1} \sin \omega\tau}{D \cos \omega\tau - 1} \right) \right] & \text{for } D^2 > 1 \\ \dfrac{1 - D}{\pi(1 - \cos \omega\tau)} \left[\omega\tau - \dfrac{D - \cos \omega\tau}{\sqrt{1 - D^2}} \tanh^{-1}\left(\dfrac{\sqrt{1 - D^2} \sin \omega\tau}{D \cos \omega\tau - 1} \right) \right] & \text{for } D^2 < 1 \end{cases} \quad (36)$$

The fundamental component of current is

$$I_{C1} = \frac{1}{\pi} \int_{-\pi}^{\pi} \cos \omega t \; I_{C,max} \left(\frac{1 - D}{1 - \cos \omega\tau} \right) \left(\frac{\cos \omega\tau - \cos \omega t}{D - \cos \omega t} \right) d(\omega t) \quad (37)$$

$$\frac{I_{C1}}{I_{C,max}} \triangleq K_5(\omega\tau, D)$$

$$= \begin{cases} \dfrac{2(1 - D)}{\pi(1 - \cos \omega\tau)} \left[\sin \omega\tau + (D - \cos \omega\tau)\, \omega\tau - \dfrac{D(D - \cos \omega\tau)}{\sqrt{D^2 - 1}} \tan^{-1}\left(\dfrac{\sqrt{D^2 - 1} \sin \omega\tau}{D \cos \omega\tau - 1} \right) \right] & \text{for } D^2 > 1 \\ \dfrac{2(1 - D)}{\pi(1 - \cos \omega\tau)} \left[\sin \omega\tau + (D - \cos \omega\tau)\, \omega\tau - \dfrac{D(D - \cos \omega\tau)}{\sqrt{1 - D^2}} \tanh^{-1}\left(\dfrac{\sqrt{1 - D^2} \sin \omega\tau}{D \cos \omega\tau - 1} \right) \right] & \text{for } D^2 < 1 \end{cases}$$

Because the functions K_4 and K_5 are so complicated, it is convenient to solve them by a computer for the expected range of α_T and D. This has been done for values of D based on γ, g_{mo}, V_{CC}, and $V_{C,min}$ typical of a wide range of transistors and operating conditions. The results are given in Fig. 20 along with the ratio K_4/K_5 which will also be useful.

The final results of the analysis are contained in the following expressions for output power, efficiency, and power gain:

$$P_L = \frac{1}{2}(V_{CC} - V_{C,min})\, I_{C1} = \frac{1}{2}(V_{CC} - V_{C,min}) K_5\, I_{C,max} \tag{39}$$

$$E_C = \frac{P_L}{P_{in,dc}} = \frac{1}{2}\frac{(V_{CC} - V_{C,min})}{V_{CC}}\frac{K_5}{K_4} \tag{40}$$

$$G = \frac{P_L}{P_{in,ac}} = \frac{\pi(V_{CC} - V_{C,min})\, K_5}{2G_1(I_{C,max})^{\alpha_1} K_3 \left(\dfrac{\frac{1}{g_{mo}} + \gamma V_{C,min}}{1 - \cos \alpha_T}\right)^{(1+\alpha_1)}} \tag{41}$$

Note that to obtain Eq. (41), Eqs. (26) and (33) have been combined to eliminate V_1 so that the final results are given as functions of output operating conditions. Equations (39) - (41) are applicable to any transistor whose parameters α_1, G_1, V_{Th}, g_{mo}, and γ are known. They give the result of operating with a certain V_{CC} and with drive and bias conditions such as to result in a certain $I_{C,max}$, $V_{C,min}$ and α_T as long as the transistor does not saturate. Once again an important special case is that in which the transistor just saturates at the extreme of the cycle. In this case $V_{C,min} = R_S\, I_{C,max}$ and the complete set of equations [analogous to (13) and (13a) for the simple model] is:

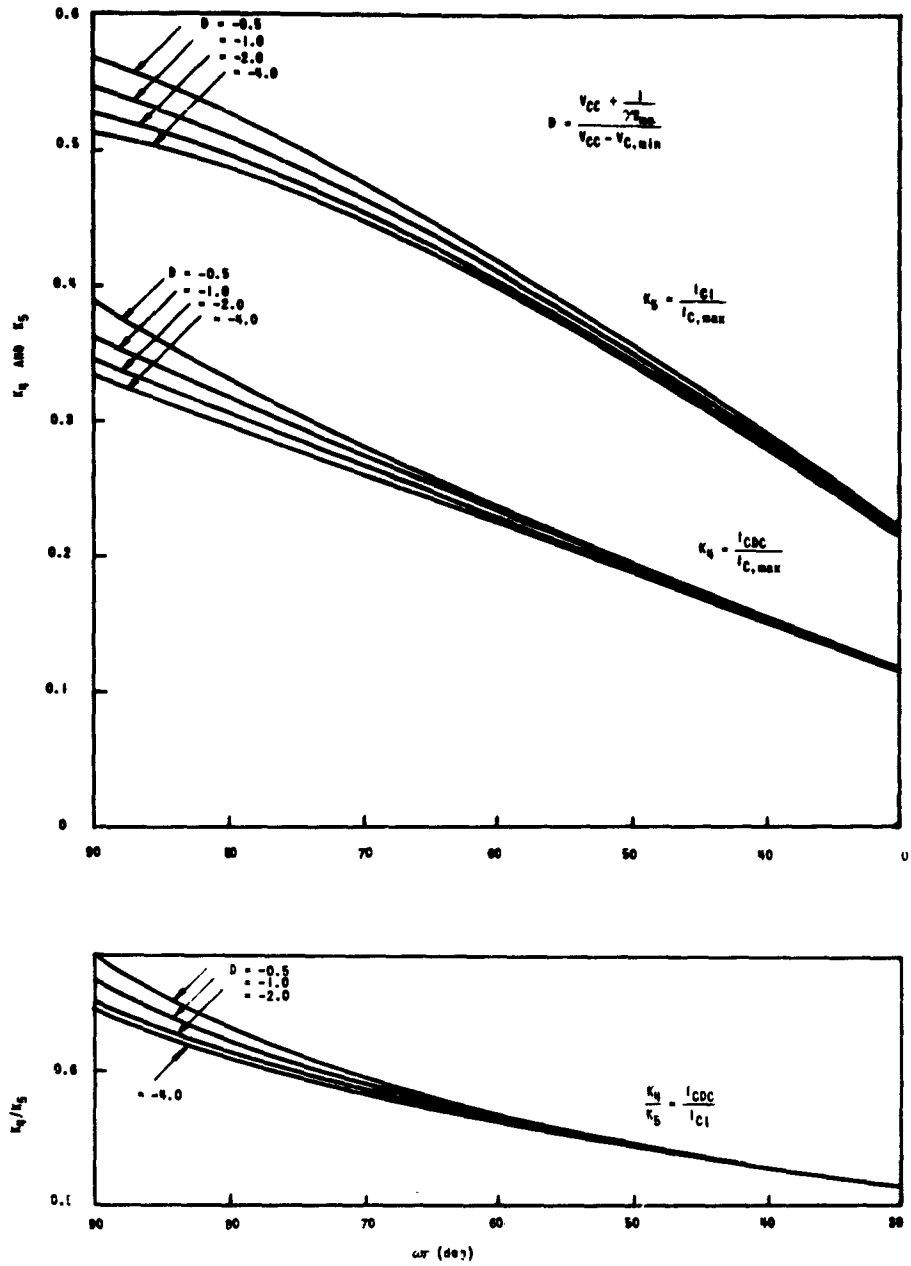


FIG. 20. VALUES OF K_4, K_5, AND K_4/K_5.

$$
\left.
\begin{aligned}
P_L &= \tfrac{1}{2}\,(V_{CC} - R_S I_{C,max})\,K_5 I_{C,max} \\
E_C &= \tfrac{1}{2}\,\frac{(V_{CC} - R_S I_{C,max})}{V_{CC}}\,\frac{K_5}{K_4} \\
G &= \frac{\omega(V_{CC} - R_S I_{C,max})\,K_5}{2G_1 K_3 (I_{C,max})^{\alpha_1}} \left(\frac{1 - \cos \omega\tau}{\frac{1}{g_{mo}} + \gamma R_S I_{C,max}} \right)^{(1+\alpha_1)}
\end{aligned}
\right\} \qquad (42)
$$

where K_3 is given in Fig. 19; K_4, K_5, and K_5/K_4 are given in Fig. 20; and

$$D = \frac{V_{CC} + \frac{1}{\gamma g_{mo}}}{V_{CC} - R_S I_{C,max}}$$

With subsidiary design equations,

$$
\left.
\begin{aligned}
R_L &= \tfrac{1}{2}\,\frac{(V_{CC} - R_S I_{C,max})^2}{P_L} \\
V_i &= I_{C,max}\,\frac{\frac{1}{g_{mo}} + \gamma R_S I_{C,max}}{1 - \cos \omega\tau} \\
V_{BB} &= V_i \cos \omega\tau - V_{Th}
\end{aligned}
\right\} \qquad (42a)
$$

Once again V_{CC} will either be specified to the designer or should be chosen as large as possible within breakdown limitations. In order to choose $I_{C,max}$ and $\omega\tau$ it is again convenient to plot P_L, E_C, and G on $I_{C,max}$ and $\omega\tau$ coordinates. Constant P_L curves are plotted by using

$$K_5 = \frac{2P_L}{I_{C,max}(V_{CC} - R_S I_{C,max})} \qquad (43)$$

where K_5 and D are calculated for various $I_{C,max}$ and the corresponding $\omega\tau$ are found from Fig. 20. Constant efficiency curves are plotted by using

$$I_{C,max} = \frac{V_{CC}}{R_S}\left(1 - 2E_C\frac{K_4}{K_5}\right) \tag{44}$$

where K_4/K_5 corresponding to a certain $\omega\tau$ is found from Fig. 20. Here it is necessary to guess in advance which D curve to use and then check to see that the value of $I_{C,max}$ obtained from Eq. (44) gives that value of D. Usually, however, $R_S I_{C,max} \ll V_{CC}$ so that the value of D is relatively independent of $I_{C,max}$.

Constant power-gain curves are plotted by using

$$\frac{K_5(1 - \cos\omega\tau)^{(1+\alpha_i)}}{K_3} = G\frac{2G_i(I_{C,max})^{\alpha_i}\left(\frac{1}{g_{mo}} + \gamma R_S I_{C,max}\right)^{(1+\alpha_i)}}{\pi(V_{CC} - R_S I_{C,max})} \tag{45}$$

Here one first plots the left-hand side vs $\omega\tau$ for the known α_i and D corresponding to a median value of $I_{C,max}$ using Figs. 19 and 20 for K_3 and K_5. Then for various $I_{C,max}$ one evaluates the right-hand side and uses the plot of the left-hand side to obtain the corresponding value of $\omega\tau$.

The operating plot for the 2N1506 transistor has been constructed and is shown in Fig. 21. The values of the transistor parameters used were

$\alpha_i = 2.27$ $\qquad$ $\gamma = -0.0064$ amp^{-1}

$G_i = 0.11$ amp/(v)$^{2.27}$ $\qquad$ $R_S = 7$ ohms

$V_{Th} = 0.67$ v $\qquad$ $V_{CC} = 40$ v

$g_{mo} = 1.15$ mhos

When Fig. 21 is compared with Fig. 8, the operating chart for the same conditions but using the simpler model, there is seen to be general agreement. The second method gives more accurate results but

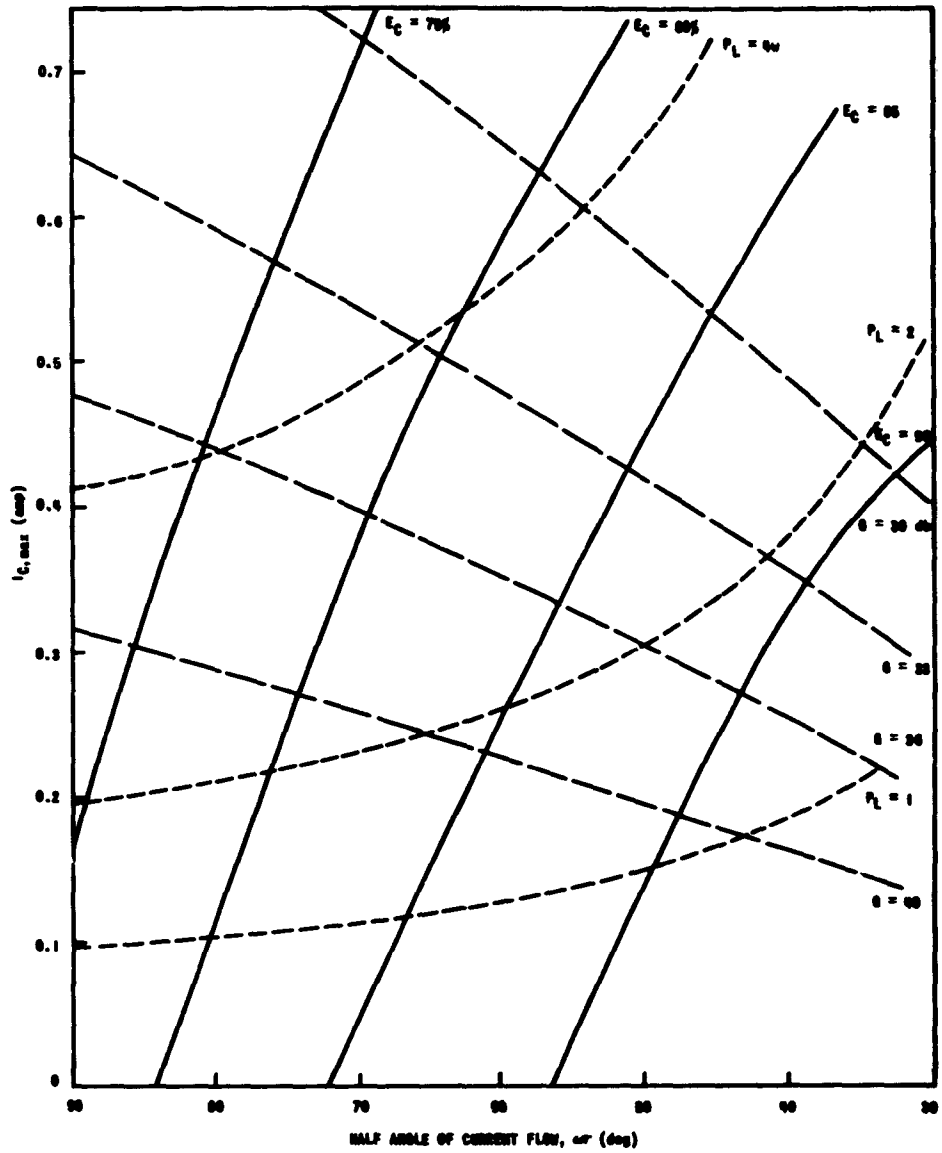


FIG. 21. OPERATING CHART FOR THE 2N1506 TRANSISTOR, SECOND ANALYSIS (V_{CC} = 40 v).

the first method evidently also gives a good approximation. This concludes the development of the analytic and design techniques for low-frequency, nonsaturating Class C amplifiers.

E. LIMITATIONS ON OPERATING CONDITIONS

There are a number of factors which limit the choice of operating condition. The first of these is collector supply voltage. Generally the maximum collector voltage specified by the manufacturer is BV_{CEO}, i.e., the open-base emitter-collector avalanche multiplication voltage. However, for Class C amplification the emitter-base junction is back biased when the collector voltage swings above the supply voltage. Moreover, the tuned circuit in the base provides practically a short circuit for direct current. Therefore, the appropriate limiting collector voltage is BV_{CES}, the shorted-base collector-emitter breakdown voltage. Since the collector voltage may swing to twice the supply voltage, the maximum supply voltage is

$$V_{CC,max} = \frac{1}{2} BV_{CES} \tag{46}$$

Once V_{CC} has been chosen, the other limitations are conveniently shown on the operating chart constructed for the chosen V_{CC}. The peak collector current is simply a straight horizontal line at the top. The transistor dissipation limit can be drawn since load power and efficiency grids are on the chart. The power one selects for maximum allowable dissipation depends on the manufacturer's ratings, the maximum ambient temperature, and the adequacy of the heat sinking. If $P_{d,max}$ is the maximum dissipated power one selects, then

$$\frac{P_{d,max}}{P_{d,max} + P_L} = E_C \tag{47}$$

describes the locus for allowable dissipation.

The final limitation is the reverse emitter-base breakdown voltage. By eliminating V_i from the last two equations in set (42a) one has

$$\frac{(V_{BB} + V_{Th})(1 - \cos \omega\tau)}{\cos \omega\tau} = I_{C,max}\left(\frac{1}{g_{mo}} + \gamma R_S I_{C,max}\right) \qquad (48)$$

If V_{BB} is set at its largest value, this equation describes a locus of $\omega\tau$ and $I_{C,max}$ corresponding to reverse emitter-base breakdown. In order to choose the maximum value of V_{BB}, one must estimate the maximum expected forward swing of the base from the emitter-base characteristics. Then one chooses V_{BB} so that the maximum swing in the other direction does not cause breakdown.

Figure 22 illustrates typical limitations on an operating chart for

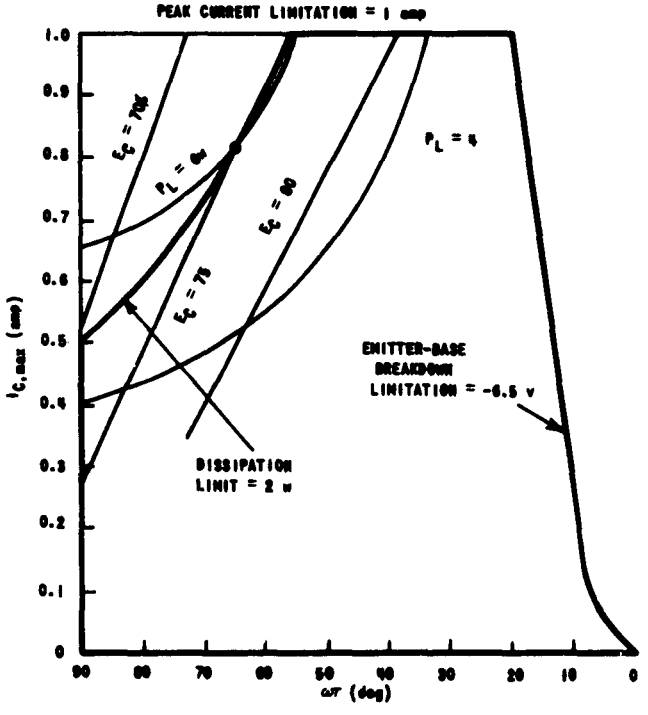


FIG. 22. LIMITS OF OPERATION FOR THE 2N1506 TRANSISTOR (V_{CC} = 40 v).

the 2N1506 transistor. Only that part of the chart necessary for determining the dissipation limit line is included to reduce the confusion slightly.

F. TEST RESULTS

To check the results of these analyses, the test circuit shown in Fig. 23 was constructed. The output tank circuit was made to be replaceable and a number of tank circuits were built, each with a different

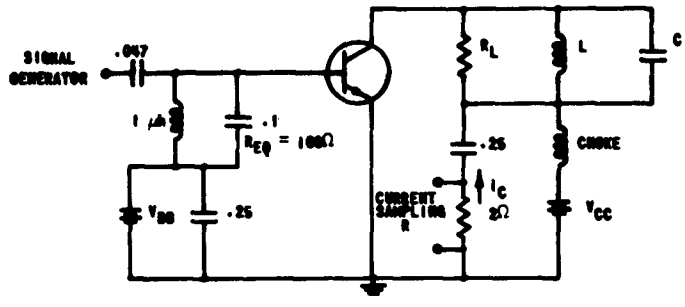


FIG. 23. LOW-FREQUENCY TEST CIRCUIT.

load resistance but with a Q of about 15. One set was tuned to 0.5 Mc as it was expected that this frequency would be low enough so that the low-frequency analysis would apply exactly. The tuned circuit in the base was made to have a loaded Q of about 15 when the maximum expected input power was being called for. Input ac power was measured by measuring the current, voltage, and phase from the signal generator using a dual-trace oscilloscope and subtracting the power known to be dissipated in the unloaded input circuit at the measured voltage. The output ac power was obtained by measuring the collector voltage with an oscilloscope and computing with the known load resistance. Input dc power was measured using dc metering on the collector supply.

For each of several load circuits V_{BB} was adjusted for several different angles of current flow, and the drive voltage was set each time to result in collector saturation at the peak of the cycle. The

collector-current waveform was observed across a small sampling resistor. This allowed the operator to set the drive voltage for saturation by observing when the collector current began to flatten at the peak. The peak collector current and the angle of current flow were also measured in this way.

The results of these measurements are given in Table 2 along with the values which would be predicted by entering the operating chart (Fig. 21) at the measured current and flow angle.

TABLE 2. MEASUREMENTS OF THE 0.5-MC AMPLIFIER FOR THE 2N1506 TRANSISTOR WITH $V_{CC} = 40$ v

Operating Condition		Load Power P_L (w)		Efficiency E_C (percent)		Power Gain G (db)	
$I_{C,max}$ (ma)	$\omega\tau$ (deg)	Predicted	Measured	Predicted	Measured	Predicted	Measured
135	75	1.25	1.22	82	80	45	30
255	80	2.3	1.93	78	77	41	34
260	36	1.3	1.2	92	93	35	29
370	51	2.4	1.9	86	82	34	29
520	29	2.0	1.6	88	78	27	23
520	56	3.6	2.7	82	68	32	29
740	34	3.3	2.8	85	73	25	23

Typical waveforms from this test are shown in Fig. 24. Note that the collector-current flow occurs only when the base voltage is above a certain value. The reason that the collector current is not constant and zero during the interpulse period is that collector-base junction charging current flows then.

In general the results of these measurements are in good agreement with the predictions. The outstanding deviation appears in the power gain where the measured gains are lower by 2 to 15 db than the predictions. These are due partly to measurement difficulty but primarily to the fact that frequency effects in the input ac power are present even at this low frequency. The output power and efficiency are also somewhat less than predicted. The primary reason for this is that the collector

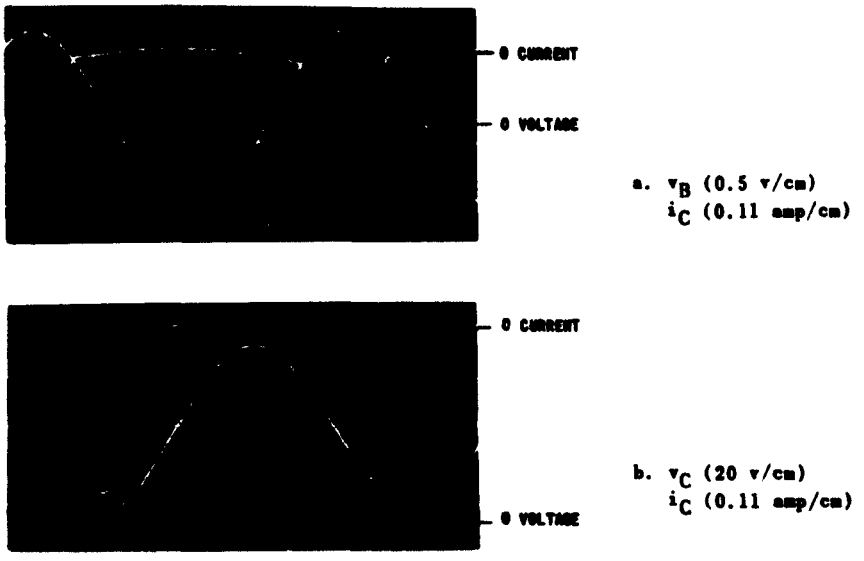


FIG. 24. WAVEFORMS FROM THE 0.5-Mc AMPLIFIER (V_{CC} = 40 v, R_L = 315Ω).

saturation resistance is affected by frequency and even at 0.5 Mc is larger than its dc value. If the operating plot had been constructed using a value of saturation resistance appropriate to 0.5 Mc the agreement would have been closer. These effects will be discussed in greater detail in Chapter V.

Table 2 shows that the efficiency at higher current levels is less than predicted. This is because the saturation point really does not follow a linear relation between the peak collector current and the minimum collector voltage.

The same tests using the same measurement methods were also performed at 3 Mc. The circuit of Fig. 23 was again used with replaceable collector tuned circuits and a base circuit tuned to 3 Mc. The results are tabulated in Table 3 and are generally the same as those noticed at 0.5 Mc. The difference between predicted and measured power gain is even more significant here due to the neglected frequency-dependent ac input power.

An operating chart was prepared for the MM487 transistor using R_S = 10Ω which was appropriate for this transistor at this frequency. Measurements were made in the same 3-Mc amplifier with the results shown in Table 4.

TABLE 3. MEASUREMENTS OF THE 3-MC AMPLIFIER FOR THE 2N1506 TRANSISTOR WITH $V_{CC} = 40$ v

Operating Condition		Load Power P_L (w)		Efficiency E_C (percent)		Power Gain G (db)	
$I_{C,max}$ (ma)	$\omega\tau$ (deg)	Predicted	Measured	Predicted	Measured	Predicted	Measured
125	90	1.3	1.01	76	76	-	-
160	78	1.5	1.48	80	71	43	28
160	64	1.3	0.96	85	83	-	-
180	51	1.2	1.14	89	86	-	-
190	64	1.6	1.46	84	73	-	-
195	48	1.3	1.00	89	88	-	-
220	51	1.5	1.43	88	75	39	25
290	42	1.6	1.39	90	77	35	21
330	77	3.0	2.07	77	68	39	27
340	70	2.9	2.14	81	71	38	27
340	35	1.7	1.31	91	76	32	19
370	57	2.7	2.12	84	72	35	25
420	47	2.6	2.16	86	71	32	23
500	85	4.6	3.6	73	60	35	26
620	69	4.8	4.08	77	68	31	23
660	65	4.8	4.23	77	70	30	21

TABLE 4. MEASUREMENTS OF THE 3-MC AMPLIFIER FOR THE MM487 TRANSISTOR WITH $V_{CC} = 40$ v

Operating Condition		Load Power P_L (w)		Efficiency E_C (percent)	
$I_{C,max}$ (ma)	$\omega\tau$ (deg)	Predicted	Measured	Predicted	Measured
27	90	2.8	2.5	70	70
31	80	2.9	2.7	74	76
34	74	3.0	2.9	75	82

This concludes the discussion of the low-frequency nonsaturating amplifier. The methods developed are evidently satisfactory for use at frequencies low compared to f_β, although the prediction of power gain is generally too large.

IV. LOW-FREQUENCY SATURATING CLASS C AMPLIFIERS

A. INTRODUCTION

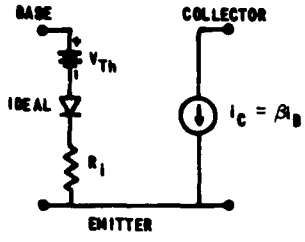
Saturating Class C amplifiers are of particular interest becuase the collector efficiency can be greater than the collector efficiency of the nonsaturating amplifier. Consequently, for the same power dissipated in the transistor, a much larger output power can be obtained. However, when the transistor is driven into saturation, the base input current rises considerably and more drive power is required. The power gain is therefore less for this type of operation. At low frequencies the gain can still be on the order of 15-20 db so that a relatively small amount of drive power may be sufficient.

The model to be used in the analysis developed in this chapter is an extension of the first model used in Chapter III and is indicated along with its characteristics in Fig. 25. Out of saturation the collector current is assumed, as before, to be a constant (β) times the base current, where the value of β depends on the maximum collector current during the pulse and has been determined along the saturation line (see Figs. 6 and 7). The transistor input is represented by a series resistor and a biased ideal diode before the saturation region is entered.

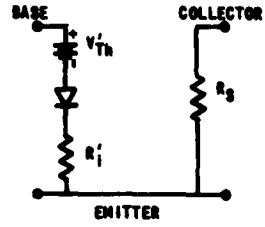
In saturation, the collector current is assumed to be a linear function of the collector voltage and the slope of the saturation line is assumed to be $1/R_S$. The base current is assumed to be linearly related to the base voltage with a slope $1/R_i'$.

The model, therefore, is the same as the first one used in Chapter III except for the change to a smaller base input resistance during saturation. Figure 26 is a plot of base current vs base voltage for various constant collector voltages. These data are the basis for the two-slope model chosen for the input. The input current-voltage relationship follows one law when the collector voltage is sufficiently high (unsaturated), and another when the collector voltage is low (saturated).

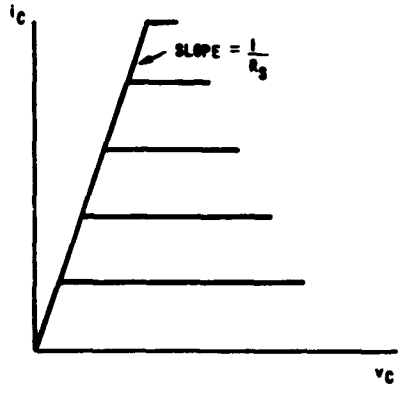
In many respects this model is not very close to the actual transistor. At high current levels particularly, the collector current is greatly dependent on collector voltage; in saturation the collector current is actually dependent on base current as well as on collector



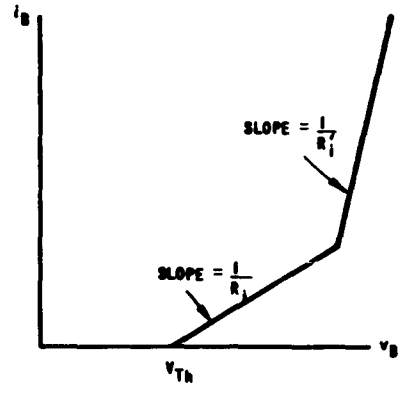
a. Nonsaturated (β is a function of $I_{C,max}$)



b. Saturated

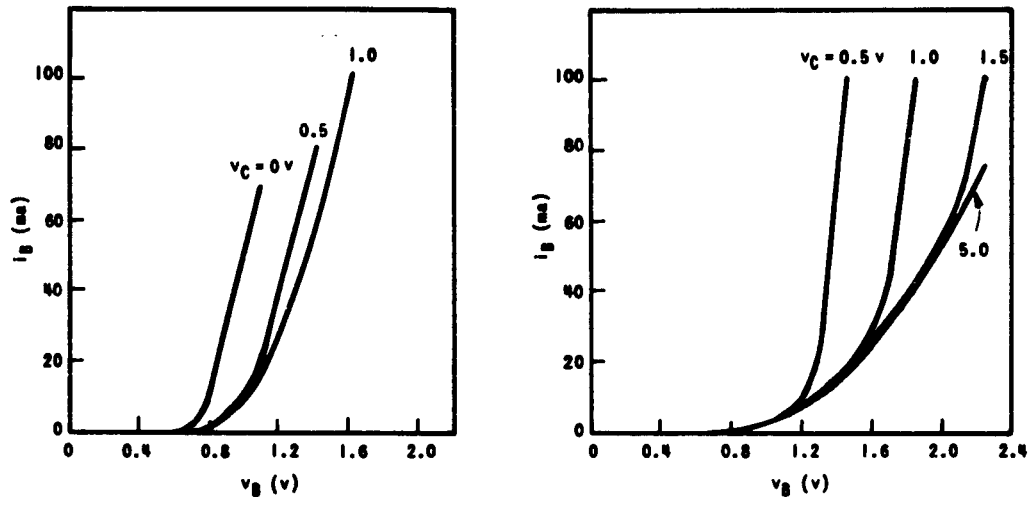


c. Collector characteristics



d. Base characteristics

FIG. 25. MODEL FOR ANALYSIS OF THE SATURATING CLASS C AMPLIFIER.



a. 2N1506 Transistor

b. MM487 Transistor

FIG. 26. EMITTER-BASE CHARACTERISTICS SHOWING THE EFFECT OF SATURATION.

voltage; and β is not constant throughout the unsaturated portion of the pulse. In these and other instances the model falls short. Nevertheless, it will be found that even this model, when analyzed, gives results that are quite complicated, so much so that it is desirable to use numerical maximizing procedures. This model does give results which are reasonably accurate for operation in saturation and it was chosen for this reason.

B. ANALYSIS OF THE MODEL

The assumption again is made that the collector and base voltages are both sinusoidal and 180 deg out of phase. Figure 27 shows a typical path of operation and the collector-current pulse for operation into saturation. The pulse is two sinusoidal sections. In the active region the collector current is β times the base current which is a sinusoidal section because the base voltage is sinusoidal and applied to a linear

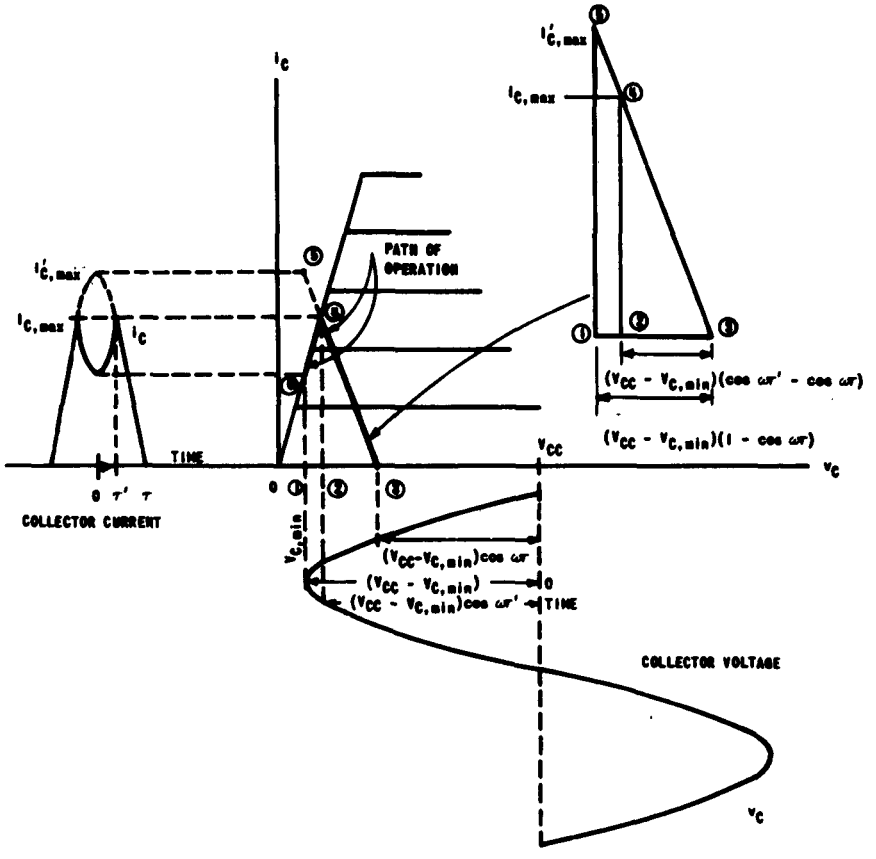


FIG. 27. APPROXIMATE COLLECTOR CHARACTERISTICS AND WAVEFORMS.

resistance. In the saturation region the collector current is a sinusoidal section because it is linearly related to the collector voltage which is sinusoidal.

The collector current is:

1. For $-\tau < t < -\tau'$ and $\tau' < t < \tau$ [see Eq. (2)]

$$i_C = \frac{I'_{C,max}}{1 - \cos \omega\tau} [\cos \omega t - \cos \omega\tau] \qquad (49)$$

Noticing in Fig. 27 that triangles ②-③-④ and ①-③-⑤ are similar, we obtain:

$$\frac{I'_{C,max}}{I_{C,max}} = \frac{1 - \cos \omega\tau}{\cos \omega\tau' - \cos \omega\tau} \tag{50}$$

When $I'_{C,max}$ is eliminated from Eqs. (49) and (50), the current becomes

$$i_C = \frac{I_{C,max}}{\cos \omega\tau' - \cos \omega\tau} (\cos \omega t - \cos \omega\tau) \tag{51}$$

2. For $-\tau' < t < \tau'$

$$i_C = \frac{v_C}{R_S} \tag{52}$$

Substituting for the saturation resistance

$$R_S = \frac{V_{CC} - (V_{CC} - V_{C,min}) \cos \omega\tau'}{I_{C,max}} \tag{53}$$

and for the collector voltage

$$v_C = V_{CC} - (V_{CC} - V_{C,min}) \cos \omega t \tag{54}$$

yields

$$i_C = I_{C,max} \frac{V_{CC} - (V_{CC} - V_{C,min}) \cos \omega t}{V_{CC} - (V_{CC} - V_{C,min}) \cos \omega\tau'} \tag{55}$$

Having the collector current and load voltage, the load power is obtained by integration of $i_C v_L$.

$$P_L = 2f\left\{\int_0^{\tau'} I_{C,max}\,\frac{V_{CC} - (V_{CC} - V_{C,min})\cos\omega t}{V_{CC} - (V_{CC} - V_{C,min})\cos\omega\tau'}\,(V_{CC} - V_{C,min})\cos\omega t\,dt + \int_{\tau'}^{\tau}\frac{I_{C,max}}{\cos\omega\tau' - \cos\omega\tau}(\cos\omega t - \cos\omega\tau)(V_{CC} - V_{C,min})\cos\omega t\,dt\right\} \tag{56}$$

Performing the integration gives

$$P_L = \frac{(V_{CC} - V_{C,min})}{\pi}\,I_{C,max}\left\{\frac{V_{CC}\sin\omega\tau' - (V_{CC} - V_{C,min})\left(\frac{\omega\tau'}{2} + \frac{\sin 2\omega\tau'}{4}\right)}{V_{CC} - (V_{CC} - V_{C,min})\cos\omega\tau'} + \frac{\frac{\omega\tau}{2} - \frac{\omega\tau'}{2} + \frac{\sin 2\omega\tau}{4} - \frac{\sin 2\omega\tau'}{4} - \cos\omega\tau(\sin\omega\tau - \sin\omega\tau')}{\cos\omega\tau' - \cos\omega\tau}\right\} \tag{57}$$

For later work let this be called $f_1(V_{C,min}, I_{C,max}, \omega\tau, \omega\tau')$.

When $\omega\tau' = 0$ this reduces to the formula for the nonsaturating case Eq. (10).

The dc power from the collector supply is obtained by integration of $i_C V_{CC}$.

$$P_{in,dc} = 2f\,V_{CC}\left\{\int_0^{\tau'} I_{C,max}\,\frac{V_{CC} - (V_{CC} - V_{C,min})\cos\omega t}{V_{CC} - (V_{CC} - V_{C,min})\cos\omega\tau'}\,dt + \int_{\tau'}^{\tau}\frac{I_{C,max}}{\cos\omega\tau' - \cos\omega\tau}(\cos\omega t - \cos\omega\tau)\,dt\right\} \tag{58}$$

Performing this integration gives

$$P_{in,dc} = \frac{V_{CC}I_{C,max}}{\pi}\left\{\frac{V_{CC}\omega\tau' - (V_{CC} - V_{C,min})\sin\omega\tau'}{V_{CC} - (V_{CC} - V_{C,min})\cos\omega\tau'} + \frac{\sin\omega\tau - \sin\omega\tau' - \cos\omega\tau\,(\omega\tau - \omega\tau')}{\cos\omega\tau' - \cos\omega\tau}\right\} \tag{59}$$

When $\omega\tau' = 0$ this also reduces to the corresponding formula for the nonsaturating case, Eq. (7).

The collector efficiency is $P_L/P_{in,dc}$ or the ratio of Eqs. (57) and (59).

The base current is:

1. For $-\tau < t < -\tau'$ and $\tau' < t < \tau$

$$i_B = \frac{V_i \cos \omega t - V_{BB} - V_{Th}}{R_i} = \frac{V_i}{R_i} (\cos \omega t - \cos \omega\tau) \tag{60}$$

2. For $-\tau' < t < \tau'$

$$i_B = \frac{V_i}{R_i} (\cos \omega\tau' - \cos \omega\tau) + \frac{V_i}{R_i'} (\cos \omega t - \cos \omega\tau') \tag{61}$$

The ac power from the source is obtained by integration of $i_B V_i \cos \omega t$.

$$P_{in,ac} = 2f \left\{ \int_0^{\tau'} \left[\frac{V_i}{R_i} (\cos \omega\tau' - \cos \omega\tau) + \frac{V_i}{R_i'} (\cos \omega t - \cos \omega\tau') \right] V_i \cos \omega t \, dt + \int_{\tau'}^{\tau} \frac{V_i}{R_i} (\cos \omega t - \cos \omega\tau) V_i \cos \omega t \, dt \right\} \tag{62}$$

Performing the integration gives

$$P_{in,ac} = \frac{V_i}{\pi} \left\{ \frac{V_i}{R_i} \left[(\cos \omega\tau' - \cos \omega\tau) \sin \omega\tau' + \frac{\omega\tau}{2} - \frac{\omega\tau'}{2} + \frac{\sin 2\omega\tau}{4} - \frac{\sin 2\omega\tau'}{4} - \cos \omega\tau (\sin \omega\tau - \sin \omega\tau') \right] + \frac{V_i}{R_i'} \left[\frac{\omega\tau'}{2} + \frac{\sin 2\omega\tau'}{4} - \cos \omega\tau' \sin \omega\tau' \right] \right\} \tag{63}$$

When $\omega\tau'$ is set to zero this reduces to the nonsaturating case, Eq. (5).

The power gain is $P_L/P_{in.ac}$ or the ratio of Eqs. (57) and (63).

Several additional equations are needed. The equation relating flow angle ($\omega\tau$) to the base bias voltage (V_{BB}), the threshold voltage (V_{Th}) and the drive voltage is

$$\omega\tau = \cos^{-1}\left(\frac{V_{BB} + V_{Th}}{V_i}\right) \tag{64}$$

The equation relating load power (P_L) to load resistance R_L, collector supply voltage (V_{CC}), and minimum collector voltage ($V_{C,min}$) is

$$P_L = \frac{(V_{CC} - V_{C,min})^2}{2R_L} \tag{65}$$

The relation between saturation resistance (R_S), collector supply voltage (V_{CC}), maximum collector current ($I_{C,max}$), minimum collector voltage ($V_{C,min}$), and half angle of saturation ($\omega\tau'$) was shown in Eq. (53).

A final equation relates the maximum collector current ($I_{C,max}$), the half angle of current ($\omega\tau$), the half angle of saturation ($\omega\tau'$), current gain (β), input resistance (R_i), and input voltage (V_i). $I'_{C,max}$ is the maximum current which would flow at the time of minimum collector voltage if saturation had not occurred.

$$I'_{C,max} = \beta I'_{B,max} = \beta \frac{V_i - V_{BB} - V_{Th}}{R_i} = \beta \frac{V_i}{R_i}(1 - \cos\omega\tau) \tag{66}$$

Equation (50) relates $I_{C,max}$ and $I'_{C,max}$. Using this with Eq. (66) gives

$$\frac{I_{C,max}}{\cos\omega\tau' - \cos\omega\tau} = \beta \frac{V_i}{R_i} \tag{67}$$

In order to analyze the results of operating with a given set of circuit conditions, Eqs. (53), (57), (59), (63), (64), (65), and (67) are needed. A given set of conditions will mean specifying V_i, R_i, R'_i, V_{BB}, V_{Th}, V_{CC}, R_L, and R_S. The problem then is to determine what set of $I_{C,max}$, β (which is a function of $I_{C,max}$), $\omega\tau$, $\omega\tau'$, and $V_{C,min}$

results. Using that set, $P_{in,ac}$, $P_{in,dc}$, and P_L, and consequently power gain and efficiency, may be calculated.

The following procedure may be followed for determining the set of $I_{C,max}$, etc., which results from a given set of circuit conditions.

1. Determine $\omega\tau$ from

$$\omega\tau = \cos^{-1}\left(\frac{V_{BB} + V_{Th}}{V_i}\right) \tag{64}$$

2. Plot a curve of $\omega\tau'$ vs $I_{C,max}$ from

$$\omega\tau' = \cos^{-1}\left[\cos \omega\tau + \frac{R_i}{V_i}\frac{I_{C,max}}{\beta}\right] \tag{67}$$

using the known function of $I_{C,max}$ for β and the value of $\omega\tau$ from step 1.

3. Plot a curve of $V_{C,}$ vs $I_{C,max}$ from

$$V_{C,min} = \frac{V_{CC} \cos \omega\tau' - V_{CC} + R_S I_{C,max}}{\cos \omega\tau'} \tag{53}$$

4. Using sets of $\omega\tau'$, $I_{C,max}$, and $V_{C,min}$ from steps 2 and 3 and the value of $\omega\tau$ from 1, determine by successive tries which set fulfills

$$P_L = \frac{(V_{CC} - V_{C,min})^2}{2R_L} \stackrel{?}{=} f_1(V_{C,min}, I_{C,max}, \omega\tau, \omega\tau') \tag{57), (65}$$

The set that results in equality is the correct set and may then be used to calculate the various powers, efficiency, and power gain.

C. TEST RESULTS

It is evident that trying to determine an "optimum" set of operating conditions for a given set of transistor parameters is a trying task. One thing which can be investigated numerically is the variation of output power, power gain, and efficiency for various drive voltages (V_i)

with all other conditions constant. Not only is this informative but it corresponds to a most practical case for experimental confirmation and for actual use.

Since in this mode of operation we are most interested in efficiency and high power, it is reasonable to select a set of conditions which are consistent with that aim. The following conditions were chosen:

V_{CC} = 40 v R_i = 14 ohms

V_{BB} = 2.5 v R_i' = 3 ohms

R_L = 152 ohms R_S = 12 ohms

V_{Th} = 0.8 v

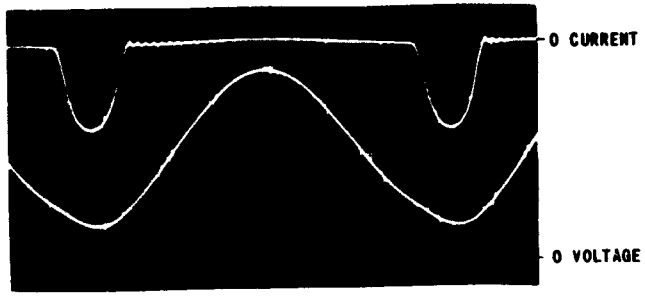
The bias voltages are near the maximum allowable for the 2N1506 transistor, R_L = 152 ohms will result in high power with the chosen V_{CC}, and the other parameters are typical of the 2N1506. R_S = 12 is typical of the saturation resistance at 0.5 Mc, the frequency at which the tests were made. (Variation of R_S with frequency will be discussed in another chapter.) The calculation procedure outlined in Sec. B was followed for a number of input voltages (V_i) which range upward from that value which just causes saturation. The results are given in Table 5.

TABLE 5. PREDICTED RESULTS OF VARIOUS DEGREES OF SATURATION

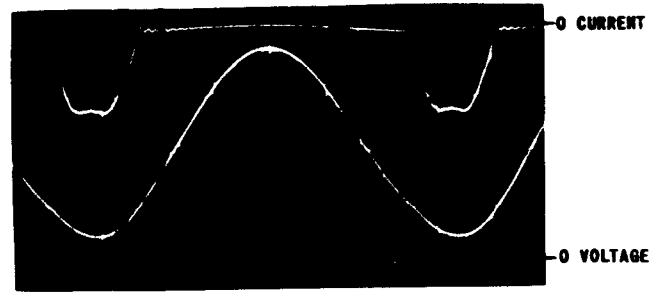
V_i (v)	$\omega\tau$ (deg)	$\omega\tau'$ (deg)	$I_{C,max}$ (amp)	$V_{C,min}$ (v)	P_L (w)	E_C (%)	G (db)
3.98	34.0	0	0.82	9.83	3.18	77	21.3
4.2	38.2	23	.77	6.6	3.67	80.6	17.3
4.4	41.4	27.5	.79	5.7	3.87	83.5	15.6
4.6	44.2	30.5	.83	5.2	3.98	78.2	14.6
4.8	46.6	32.4	.87	5.0	4.03	71.3	13.2

The measured results of a 2N1506 transistor operated under these same conditions are given in Table 6 and may be compared to those of Table 5. Waveforms from the test for various drive voltage amplitudes are shown in Fig. 28. V_i was not recorded but was calculated using

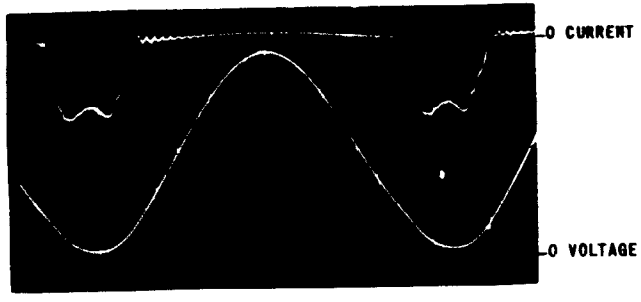
$$V_i = \frac{(V_{BB} + V_{Th})}{\cos \omega\tau}$$



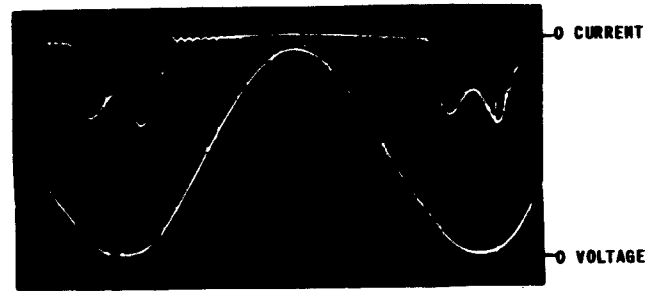
a. Drive just to saturation
P_L = 2.8 w, E_C = 73%, G = 25 db



b. Drive into saturation (flat-topped i_C)
P_L = 3.9 w, E_C = 82%, G = 23 db



c. Drive into saturation (15% dip i_C)
P_L = 4.6 w, E_C = 90%, G = 22 db



d. Drive into saturation (30% dip i_C)
P_L = 4.8 w, E_C = 88%, G = 20 db

FIG. 28. OPERATION WITH VARIOUS DEGREES OF SATURATION. Collector current (upper waveform) = 0.48 amp/cm; collector voltage = 20 v/cm; 2N1506 Transistor, V_{CC} = 40 v, R_L = 152Ω, V_{BB} = 2.5 v, f = 0.5 Mc.

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TABLE 6. MEASURED RESULTS OF VARIOUS DEGREES OF SATURATION

V_i (v)	$\omega\tau$ (deg)	$\omega\tau'$ (deg)	$I_{C,max}$ (amp)	$V_{C,min}$ (v)	P_L (w)	E_C (%)	G (db)
4.08	36	0	0.75	10.8	2.8	73	25
4.51	43	19	.70	7.0	3.9	82	23
4.84	47	22	.70	2.6	4.6	90	22
5.03	49	28	.73	1.8	4.8	88	20

from the values of $\omega\tau$ measured in the photographs of Fig. 28.

The calculated and measured results show reasonable agreement considering the approximations made and the accuracy of measurement. The theoretical approach indicates a maximum efficiency of about 84 percent occurring when $\omega\tau' \tilde{=} 26$ deg with $P_L \tilde{=} 3.8$ w and $G \tilde{=} 16$ db. The measurements indicate a maximum efficiency of about 90 percent occurring when $\omega\tau' \tilde{=} 23$ deg with $P_L \tilde{=} 4.6$ w and $G \tilde{=} 22$ db.

The largest source of error is probably the assumption that the collector current is independent of base current in saturation. This assumption results in a deeper dip of collector current than actually occurs. For instance, Fig. 28c shows a collector current dip of 15 percent of $I_{C,max}$, whereas the data of Table 5 for $V_i = 4.8$ v would indicate a dip of 50 percent. This error in the current occurs when the load voltage is maximum, thus resulting in too low predicted output power and efficiency.

V. HIGH-FREQUENCY OPERATION

A. INTRODUCTION

In the previous chapters we were able to obtain reasonably exact expressions for the operation of Class C amplifiers at low frequencies. Unfortunately, at high frequencies even a reasonably exact analysis is so complicated that it is not worthwhile. It is possible, however, to discuss in some detail the various effects that are important and thus gain an intuitive understanding of the course of proper design. It is also possible to make some rather crude assumptions and so obtain some analytic results which further aid in design. In addition a new method of analog simulation of a transistor is presented which takes into account the two-dimensional character of the transistor, the major non-linearities, the capacitive and frequency cutoff effects, and which also includes simulation of the forward-biased collector junction.

In Chapters III and IV the analysis was based strictly on the transistor current-voltage characteristics. Here it is necessary to examine the internal workings of the transistor and to be particularly concerned with the geometry. The simplest geometry to consider is the long-stripe geometry shown in Fig. 1. It is assumed that the length is enough that currents flow only in cross-sectional planes. Because the geometry is symmetrical, no currents flow across the plane of symmetry. Figure 29

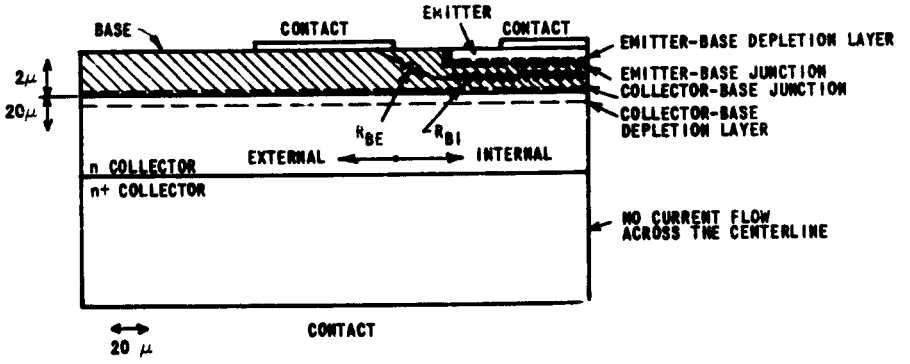


FIG. 29. CROSS SECTION OF HALF OF THE 2N1506 TRANSISTOR HAVING LONG SYMMETRICAL STRIPE GEOMETRY.

is a cross section of half of the 2N1506 transistor. In order to show some detail in the emitter and base regions, the vertical scale of the drawing was changed at the collector-base junction. In the rest of this report the vertical scale will be similarly variable in order to show the essential features in question.

The effects which are important for large-signal high-frequency operation are connected with the following:

1. Base Resistance. Because of the narrow base width, the base sheet resistivity is rather high in that part of the base lying under the emitter. The sheet resistance is typically 1,000 to 3,000 ohms. In the rest of the base the sheet resistance is much less because of the greater width and the higher doping at the surface resulting from the diffusion process. Even so, this portion of the base also contributes a significant resistance. The term "external" will apply to that portion of the transistor not under the emitter. The term "internal" will apply to that portion of the transistor under the emitter.
2. Capacitance. Depletion layer capacitances are present at emitter-base and collector-base junctions. The emitter capacitance is quite large, typically 50 to 400 pf. The collector capacitance is typically 4 to 20 pf. The edge of the collector depletion region is shown in Fig. 29 for a collector voltage of 40 v.
3. Collector Bulk Resistivity. The n collector is a region of relatively high resistivity. Carriers must flow across this region from the edge of the collector depletion region to the n+ collector and the resulting ohmic drop causes the major part of the saturation voltage.

Figure 30 is an equivalent circuit model for drive signals small enough that significant emission does not occur. The model also applies during the off portion of the cycle for larger drive voltages and it is convenient for visualizing many of the effects to be discussed. R_{BE} is the resistance between the base contact and a point in the base under the emitter edge; R_{BI} is the total resistance between the center of the base and that same point (see Fig. 29). Likewise, C_{CE} is the "external" portion of the collector depletion capacitance and C_{CI} is the "internal" portion. R_C is meant to symbolize the distributed resistance of the n collector. Although a finite number of elements are shown in the drawing, C_E and C_{CI} are both distributed capacitances.

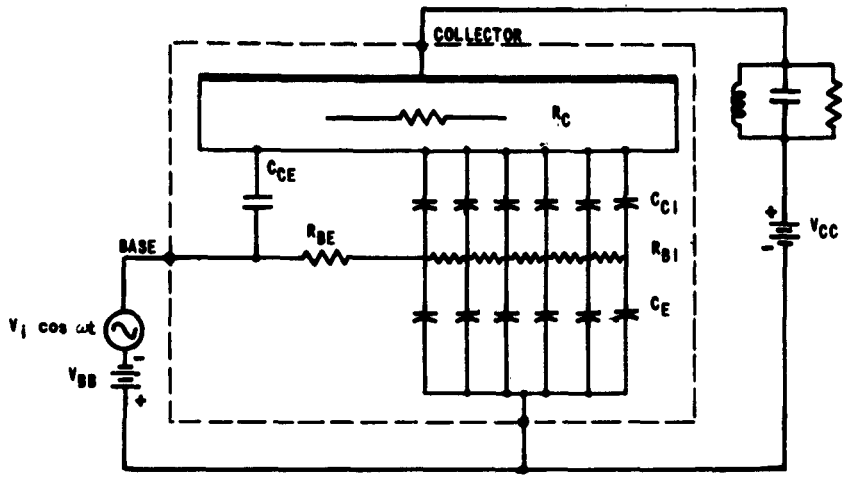


FIG. 30. EQUIVALENT CIRCUIT FOR THE GEOMETRY OF FIG. 29. Peak emitter junction voltage less than V_{Th}.

B. IMPORTANT EFFECTS OCCURRING AT HIGH FREQUENCIES

1. Current Crowding

This effect was first discussed in detail by Fletcher [Refs. 4 and 5] for the dc case. He showed that base current flowing laterally through the base resistance produces a voltage drop which reduces the forward bias voltage applied to the emitter-base junction. Because the reduction is greatest for that part of the emitter farthest from the edge, the emitter current density is greatest at the emitter edge. Mead [Ref. 6] has analyzed the dc effect, including certain results in saturation, for alloy junction transistors where he was able to neglect collector resistivity.

Even at fairly moderate current levels the emitter current density at the edge can be 100 times that at the center of the emitter. This dc current crowding is present in the static characteristics used in Chapter III and is fully taken into account there.

In Class C high-frequency operation, further effects cause emitter current crowding. Consider the transistor to be operating in

the grounded emitter configuration with a signal voltage applied to the base. Suppose this voltage is not quite enough to cause significant emission. Then the voltage appears to be applied to an open-end RC transmission line where the series resistance is the internal base resistance and the shunt capacitance is the sum of the emitter depletion capacitance, C_E, and C_{CI}. This line acts something like a low pass filter causing the amplitude of the signal voltage to decrease toward the center of the emitter. If the applied voltage is increased, further crowding effects occur when emission starts. Charge storage occurs in the base region, which has the effect of another shunt capacitance in the RC line. Finally, base current flows laterally causing a bias effect as described in the dc case.

2. Transistor Saturation

This occurs when the voltage "applied" to any part of the collector junction falls to zero. In low-level operation where the emitter current density is nearly uniform, the current emerges from the collector depletion layer and flows through the high-resistivity collector region nearly uniformly (there is some spreading into the "external" region). This results in only a very small lateral voltage gradient in R_C and since the lateral voltage drop in the base is also not very much, the effect as the collector voltage is decreased is that the entire collector junction saturates at the same time. Further increase in the base drive does not significantly affect the collector current.

When the current levels are high or the frequency is high, emitter crowding occurs so that the current emerging from the collector depletion region is no longer uniform. The current is quite dense under the emitter edge and therefore causes a large voltage gradient there. As the current flows across the high-resistivity region it spreads out so that the gradient is smaller and more uniform at the n:n+ boundary. This is indicated in Fig. 31 where lines of current have been drawn for typical current crowding in an n collector region. The main effects are (a) the maximum voltage drop across R_C occurs under the emitter edge and (b) the maximum voltage across R_C per unit total current is much larger. Now as the collector voltage is decreased, the voltage applied to the collector junction becomes zero first under the emitter edge. If the

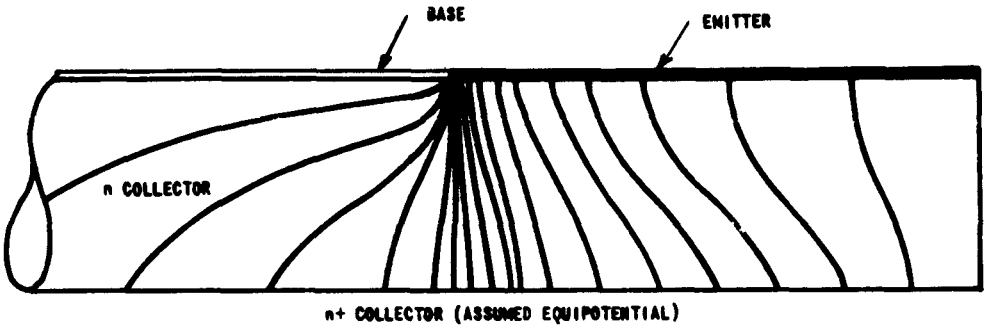


FIG. 31. PARTIAL CROSS-SECTIONAL VIEW INDICATING THE DISTRIBUTION OF CURRENT.

collector voltage is further decreased it is now possible by increasing the base drive to maintain the same collector current. What has happened is that the collector junction has become progressively forward biased. The portion under the emitter edge is more forward biased, while the division between forward and reverse-biased junction has moved in towards the center of the transistor. The significantly larger base current is due to high recombination in the base near the forward-biased portion of the collector.

The point at which saturation begins has been measured using the circuit shown in Fig. 32. For zero base bias voltage, a sine-wave voltage with constant peak amplitude was applied to the base. The collector was essentially shorted to ground through a small current-sampling resistor. In order to minimize lead inductance, the circuit was built in a GR coaxial mount. A sampling oscilloscope was used for measuring collector current and for monitoring base and collector voltages. As an example, curves of peak collector current vs collector voltage for various constant base drive voltages are shown in Fig. 32 for dc and 12 Mc. Note that the knee for the low current dc curve is quite sharp indicating simultaneous forward biasing of the entire collector junction, whereas at higher currents and high frequency the knee becomes less and less well defined indicating a gradual change from reverse to forward biasing of the collector junction.

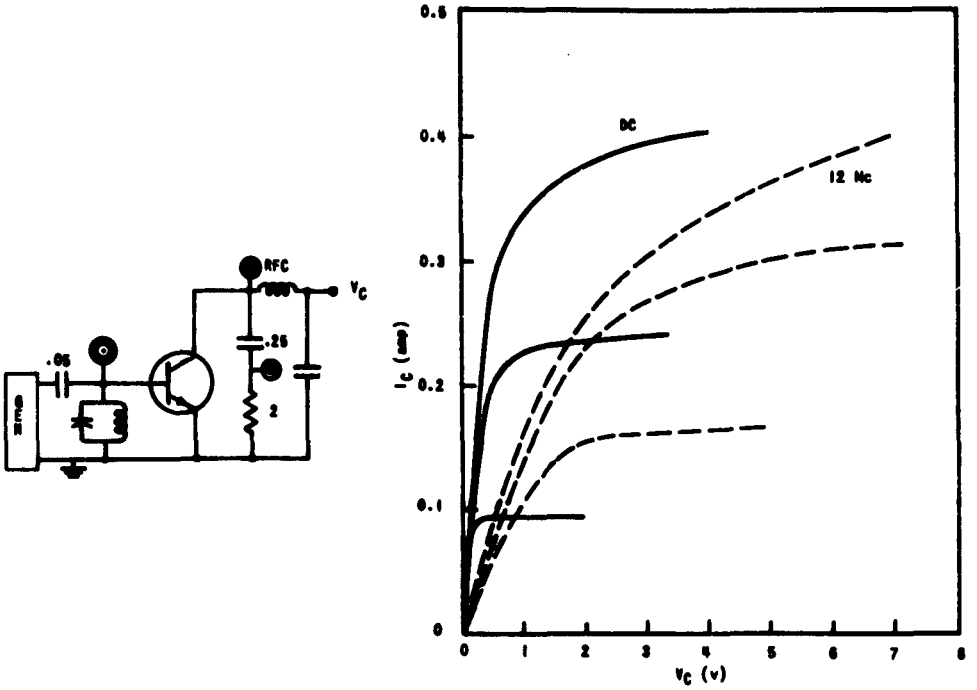


FIG. 32. DETERMINATION OF COLLECTOR SATURATION AT VARIOUS FREQUENCIES.

If the upper knee of each constant base voltage curve is taken as the point where collector saturation started, then curves of current vs voltage at initial saturation can be obtained. These are shown in Fig. 33 for a number of frequencies up to 18 Mc. (Above 12 Mc the current-sampling resistor was replaced by a current probe.) Average values of R_S are shown corresponding to the various frequencies. If one were interested in a certain frequency, an operating chart as developed in Chapter III could be prepared using the appropriate value of R_S. This would give good results for predicting output power and efficiency as a function of current and flow angle. Another method must be developed for predicting power gain and for relating collector currents and flow angles to the bias and drive conditions. As the saturation resistance becomes larger, it is more desirable to operate not just to saturation but well into it, as demonstrated before.

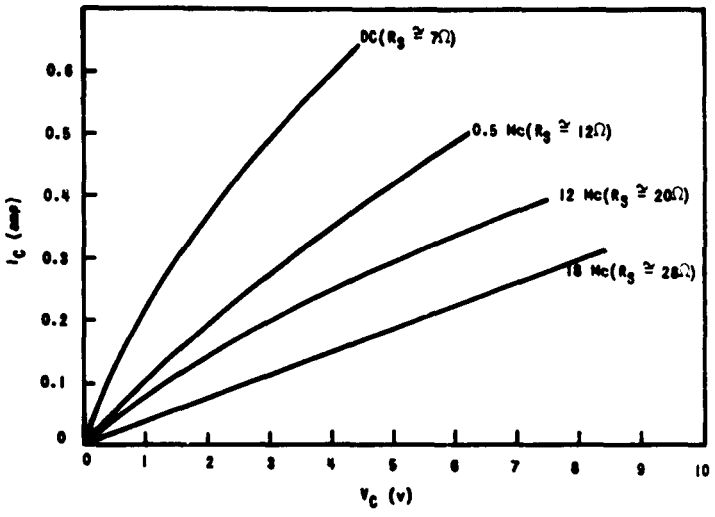


FIG. 33. INITIAL COLLECTOR SATURATION AT VARIOUS FREQUENCIES.

The fact that the collector current is most dense where it emerges from the collector depletion region means that the collector resistivity is most important there. Unfortunately, the doping profiles invariably go from low resistivity at the collector contact to higher and higher resistivity as the collector junction is approached. Therefore the current is most dense where the resistivity is highest. Transistors made by the exitaxial process attempt to remedy the situation by making the n collector width very narrow, 4-10 microns, and the resistivity very high, 100-200 ohm-cm. If the doping profiles were ideal, the collector depletion region could extend all the way across the high-resistivity portion even for quite small collector voltages. In this case, however, the space charge limiting effect described by Early [Ref. 7] may come into play where the depletion-layer bound charge is neutralized by carriers in transit.

3. Collector-Current Stretching

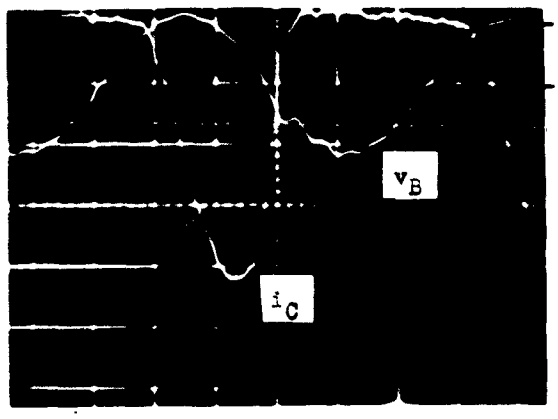
In low-frequency operation it was possible to assume that current flow began when the base voltage exceeded a certain threshold, V_{Th},

and stopped when the base voltage again fell to that threshold. This is evident in the waveforms of Fig. 24a.

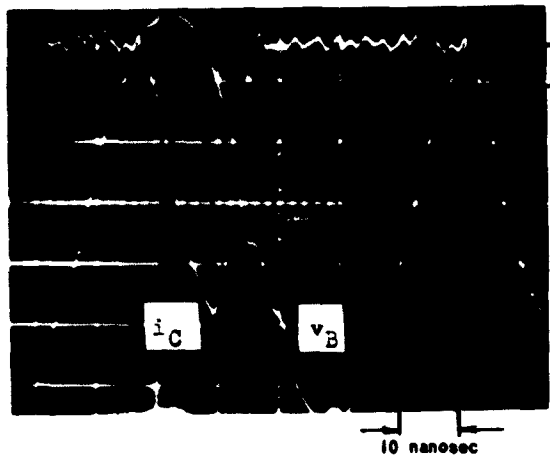
When the equivalent circuit of Fig. 30 is considered in connection with high-frequency operation, it is apparent that because of R_{BE} and the shunt capacitance of the RC line, the base voltage must rise to a somewhat larger value before the voltage at the line rises to the threshold. A much more important effect occurs when the base voltage is decreasing. During conduction the bound charge in the emitter depletion layer is at a low value and the base is filled with emitted electrons and the holes necessary to maintain charge neutrality. Before the emitter junction voltage can all be returned to the threshold and so stop the emission, the base lead must remove the charge neutralizing holes in the base and also holes from the edge of the depletion region. A significant amount of time is required to do this; in the meantime, the lateral flow of holes toward the base contact results in a voltage drop in R_{BE} and R_{BI} which maintains the emission. The net result is that at higher frequencies it becomes increasingly difficult to cause the small current flow angles which give high efficiency.

A second source of collector-current stretching is diffusion of carriers while in transit through the base. That is, if an impulse of current were emitted into the base, it would have nonzero width as it came out the collector. Even after the emitter junction is back biased so that emission stops, the excess electrons remaining in the base must be collected. Most of them will be retrieved by the now back-biased emitter, but some will be taken by the collector. The time involved here is of the order of $1/\omega_\alpha$ and so will not become important until very high frequencies are reached.

Collector-current stretching is illustrated in Fig. 34 where collector current and base voltage are shown on a dual-trace oscilloscope. The waveforms were taken using a current probe with constant collector voltage and a peak collector current less than saturation. The drive was adjusted for the same peak current in each case. It is evident that the current starts when the voltage is very near the threshold but does not stop until much later. The actual current flow angles ($\omega\tau$)



a. $V_{BB} = 0$ v
$\omega\tau = 80°$
$\omega\tau_{v_B} = 46°$



b. $V_{BB} = 2.3$ v
$\omega\tau = 62°$
$\omega\tau_{v_B} = 33°$

FIG. 34. COLLECTOR-CURRENT STRETCHING 2N1506 Transistor at 18 Mc and $V_C = 8$ v.

are compared with those which would have resulted if current stopped at the same v_B at which flow started ($\omega\tau_{v_B}$).

Although no waveforms were taken to show the effect, operation, with part of the collector forward biased results in even more stretching since there is more stored charge to remove from the base.

Besides reducing the efficiency, the stretched collector current causes the collector voltage to lag the base voltage by more than 180

deg because proper tuning of the output circuit causes the minimum collector voltage to occur approximately when the collector current is maximum. The additional lag of the collector voltage has no particularly bad effect but it prevents us from assuming that collector and base voltages are exactly out of phase as we did in Chapter III.

4. Junction Charging Current Losses

Emitter and collector voltages swing over a wide range. The current required to charge and discharge the junction capacitances flows in and out of the base lead through R_{BE} and partially through R_{BI}. In doing so, a power loss occurs which increases with frequency. For a constant waveform of current and constant total charge transported per cycle, the power lost in a series resistance is proportional to the square of the frequency. At low frequencies this is the situation. The entire emitter junction has the full base voltage across it, while the entire collector junction has the difference between base and collector voltage across it. Therefore, a certain total charge flows in and out the base lead regardless of frequency until a certain critical frequency is reached. There the distributed RC line begins to cut off and prevent the applied base voltage from reaching the interior of the line. As the frequency increases further, the power loss eventually increases at a rate intermediate between F and $\sqrt{F}$. The major part of this loss is supplied by the drive source and constitutes a large part of the required input ac power. Neglecting this contribution to input power was one of the main sources of error in power gain noticed in the test results in Chapter III.

5. Base Charging Current Losses

When the emitter injects electrons into the base, charge neutrality requires that a nearly equal number of holes flow from the base contact into the base. Once the collector current has reached a steady state, no more base charging current is required. When the pulse is to be terminated, the base hole charge must be withdrawn through the base contact. To the extent that this base charging current is withdrawn at a lower voltage than it is inserted, there is power required from the drive source. Another way of thinking of this is that the charge is

forced in and out of the base through the base resistance, thus producing a power loss.

The junction charging losses described in paragraph 4 depend on the depletion-layer charge transported which is related to the swing of the input and output voltages. This charge is relatively independent of the collector current to which the transistor is driven. For example, if V_{BB} = 2.5 v, a base voltage swing of 6.6 v peak to peak produces a peak collector current of 0.1 amp, while 7.6 v peak to peak produces a peak collector current of 0.8 amp. For zero bias the comparison is less striking, of course. There, 1.6 v peak to peak produces 0.1 amp while 2.6 v peak to peak produces 0.8 amp.

The base charging losses, on the other hand, depend primarily on the peak collector-current level and not the voltage swing because the base charge required is directly proportional to the collector current as long as flow is by diffusion only.* (It may be shown that this is true regardless of the degree of crowding.) A certain collector current requires that a certain base charge be transported through a certain base resistance so that the power lost depends on the collector current.

Let us summarize the sources of input ac power. They are,

a. Base current due to bulk and surface recombination and emitter inefficiency. This is the source accounted for in Chapter III and IV and is the only source effective at very low frequency. According to the data of Chapter III, 500 kc is still not a low enough frequency for this to be the only effective term in the transistors tested.

b. Junction charging losses. These depend on the voltage swings and increases as F^2 at low frequencies and as F or $\sqrt{F}$ at higher frequencies.

c. Base charging losses. These depend on the peak collector current and vary in the same way as junction charging losses with frequency. The critical frequency separating variation as F^2 from variation as F or $\sqrt{F}$ is much lower than that for the junction charging losses.

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*Although vhf power transistors have graded bases, the most important operation is at current levels where the built-in field is swamped out by injected carriers resulting in flow by diffusion.

In the analyses which follow it will be assumed that source a is completely negligible and that sources b and c can be separately calculated (each in an approximate way) and added, in spite of the fact that they arise in the same circuits.

6. Collector Capacitance Feedback

It is apparent from the equivalent circuit of Fig. 30 that the collector capacitance provides a feedback path. C_{CE} would not actually cause any voltage to be developed at the input if the source truly had zero impedance; however this is not usually the case, and therefore neutralization may be necessary. The position of C_{CE} allows the use of neutralization by an inductor (and a dc blocking capacitor) placed from the collector to base. Tuning the inductor to resonate with C_{CE} at the frequency of operation removes this source of feedback.

The internal part of the collector capacitance, C_{CI}, cannot very well be neutralized since it cannot be reached. Fortunately it is quite small compared with C_E. Nevertheless, some interesting possibilities occur here. Consider operation at quite high frequency, such that the voltage applied at the base is not reaching the open end of the RC line at all. Then the collector voltage is divided in the capacitance divider C_{CI} and C_E and appears across the emitter at the open end of the line along with V_{BB}. Depending on the divider ratio, the amplitude of the collector voltage swing, and the bias, the possibility exists that the central portion of the emitter could be turned on by this feedback. If the central emitter were turned on, then, collector current would occur at the time when the collector voltage was maximum, thus resulting in removal of power from the load and high dissipation in the transistor.

The transistor geometry determines how the collector capacitance is divided between C_{CE} and C_{CI}. In the 2N1506 transistor, C_{CI} is only 26 percent of the total, whereas in the TA2084 and the SN102 transistors it is 50 percent of the total. This splitting of the collector capacitance may explain why some investigators have found the common base configuration a more stable one for small-signal work with mesa and planar transistors. In that configuration C_{CE} merely shunts the output and does not contribute to feedback.

C. ANALYTIC APPROACHES

The equivalent circuit of Fig. 30 is valuable in understanding some of the effects. However, it would not be reasonable to attempt an exact analysis using this circuit during the off period, using another circuit during the on period, and then trying to determine the on and off periods by matching end-points. This would be further complicated by the fact that the on and off periods would vary from one point to another in the base and one would not know the correct phase relation between the base voltage and collector voltage to start with. The model is probably not worth exact solution since a number of complicating factors have not even been considered. (For instance, conductivity modulation of the base at high local injection densities causes R_{BI} to be variable.)

This section presents the results of an analysis of a linear open-ended RC transmission line having constant elements. We show how the line constants can be measured and how these results can be used to estimate how the transistor operates at various frequencies. In particular, the input power required to charge and discharge the junction is calculated in this way. The justification for using a constant element RC line, besides the fact that a solution can be obtained for that case, is that the junction charging current does approximate a sine wave crudely at low frequencies. As the frequency increases, the voltage at the internal portions of the emitter decreases, resulting in more nearly sinusoidal current flow.

In Appendix A a differential equation is developed, but not solved, which takes into account the nonlinear nature of the depletion capacitances and the effect of the collector voltage through C_{CI}. Except for neglecting R_C it is a good representation of the model.

In Appendix B an analysis is made of an RC transmission line having circular geometry and constant elements. This is useful when considering transistors such as the emitter dot type which have this kind of geometry.

Let us show what the base current waveform is when the frequency is low and the drive voltage is not quite enough to cause emission. Measurements of the different transistors studied have shown that the emitter capacitances vary inversely as the voltage to the 0.35 to 0.40 power

with a built-in field of about 0.8 v. The form of the capacitance-voltage function is therefore

$$C_E \cong \frac{A_E}{(V + 0.8)^{0.37}} \tag{68}$$

where A_E is a constant and V is the reverse voltage applied to the junction $(V = v_B)$. Because $C_{CI} + C_{CE}$ is usually 10 percent of C_E or less, let us assume that the base current is due entirely to C_E. The base current is then

$$i_B = -\frac{dQ_E}{dt} = -\frac{dQ_E}{dV}\frac{dV}{dt} = C_E\frac{dv_B}{dt} \tag{69}$$

If $v_B = V_i \cos \omega t - V_{BB}$,

$$i_B = \frac{-A_E V_i \omega \sin \omega t}{(V_{BB} + 0.8 - V_i \cos \omega t)^{0.37}} \tag{70}$$

This is plotted in Fig. 35 for $V_{BB} = 2.5$ and $V_i = 3.1$, i.e., for

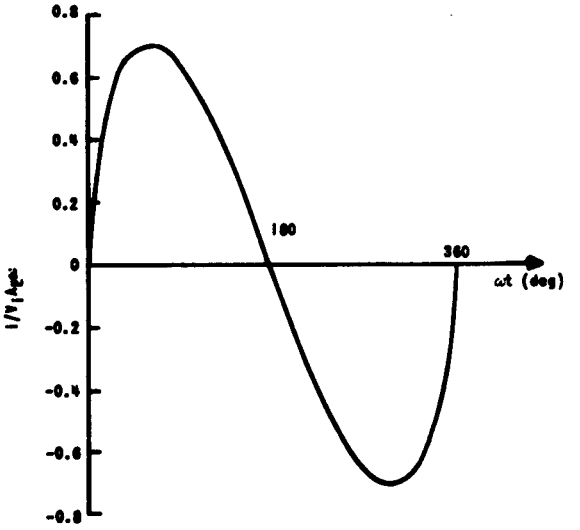


FIG. 35. JUNCTION CHARGING CURRENT WAVEFORM FOR $V_{BB} = 2.5$, $V_i = 3.1$.

bias and drive conditions such that the emitter swing approaches significant conduction at one extreme and approaches breakdown at the other. This is the largest swing that can occur and it produces the most nonlinear result. Even so, a sine-wave approximation seems justified.

If the collector voltage were also swinging, a significant part of the total junction charging current flowing in and out of the base would be due to collector junction charging because the larger voltage across the junction compensates for the lower capacitance. The collector capacitance of all the transistors is more constant than the emitter capacitance and the junction voltage does not go as far positive (if it goes positive at all) as does the emitter junction. Therefore the current would be more nearly a sine wave if the collector voltage swing were also considered.

1. Analysis of Linear Distributed RC Transmission Line with Constant Elements

Assume that we have a line of length X as shown in Fig. 36.

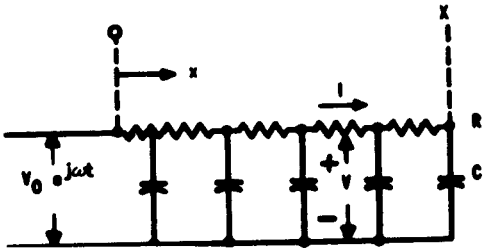


FIG. 36. RC TRANSMISSION LINE.

It has a total series resistance R and a total capacitance C. Let the voltage V and current I be as shown. The applied voltage at $x = 0$ is $V_0 \mathrm{Re}\ e^{j\omega t}$.

The differential equations are

$$\frac{\partial V}{\partial x} = - I \frac{R}{X} \tag{71}$$

and

$$\frac{\partial I}{\partial x} = - \frac{C}{X} \frac{\partial V}{\partial t} \tag{72}$$

When the first equation is differentiated and substituted in the second, we have the following partial differential equation,

$$\frac{\partial^2 V}{\partial x^2} = \frac{RC}{X^2} \frac{\partial V}{\partial t} \tag{73}$$

with boundary conditions

$$V(0,\ t) = V_0 \mathrm{Re}\ e^{j\omega t} \tag{74}$$

and

$$\frac{\partial V}{\partial x}(X,\ t) = 0 \tag{75}$$

Since we are interested only in a steady-state solution, the initial conditions are not necessary. Assume a solution of the form

$$V(x,\ t) = V_1(x)\ \mathrm{Re}\ e^{j[\omega t + \theta(x)]} \tag{76}$$

When (57) is substituted in (54) and simplified, we have (dropping the symbol Re for the time being) the ordinary differential equation

$$\frac{d^2(V_1 e^{j\theta})}{dx^2} = \frac{RC}{X^2} j\omega (V_1 e^{j\theta}) \tag{77}$$

Assuming a solution $(V_1 e^{j\theta}) = e^{px}$ gives

$$p^2 = j\omega \frac{RC}{X^2} \tag{78}$$

or

$$p = \pm(1 + j) \sqrt{\frac{\omega RC}{2X^2}} = \pm(1 + j) \frac{1}{L} \tag{79}$$

$$L \triangleq \sqrt{\frac{2X^2}{\omega RC}}$$

The solution is then

$$V_1 e^{j\theta} = A \exp\left[(1 + j)\frac{x}{L}\right] + B \exp\left[-(1 + j)\frac{x}{L}\right] \tag{80}$$

When the boundary conditions are applied and the results simplified we have

$$V_1 e^{j\theta} = V_0 \frac{\cos \frac{X-x}{L} \cosh \frac{X-x}{L} + j \sin \frac{X-x}{L} \sinh \frac{X-x}{L}}{\cos \frac{X}{L} \cosh \frac{X}{L} + j \sin \frac{X}{L} \sinh \frac{X}{L}} \tag{81}$$

The magnitude of (81) is V_1 and the angle of (81) is θ.

$$V_1 = V_0 \sqrt{\frac{\cosh 2\left(\frac{X-x}{L}\right) + \cos 2\left(\frac{X-x}{L}\right)}{\cosh \frac{2X}{L} + \cos \frac{2X}{L}}} \tag{82}$$

$$\theta = \tan^{-1}\left[\frac{\cos \frac{X}{L} \cosh \frac{X}{L} \sin \frac{X-x}{L} \sinh \frac{X-x}{L} - \sin \frac{X}{L} \sinh \frac{X}{L} \cos \frac{X-x}{L} \cosh \frac{X-x}{L}}{\cos \frac{X}{L} \cosh \frac{X}{L} \cos \frac{X-x}{L} \cosh \frac{X-x}{L} + \sin \frac{X}{L} \sinh \frac{X}{L} \sin \frac{X-x}{L} \sinh \frac{X-x}{L}}\right] \tag{83}$$

The driving point impedance is found from

$$Z = \frac{V}{I}\Big|_{x=0} \tag{84}$$

where $V(0, t) = V_0 e^{j\omega t}$ was an assumption. The current is obtained from Eq. (71).

$$I(0, t) = -\frac{X}{R} \frac{\partial V}{\partial x}(0,t) \tag{85}$$

After a good deal of algebraic manipulation and use of the hyperbolic equivalences

$$\left.\begin{aligned} \sinh (x \pm iy) &= \sinh x \cos y \pm i \cosh x \sin y \\ \cosh (x \pm iy) &= \cosh x \cos y \pm i \sinh x \sin y \end{aligned}\right\} \tag{86}$$

we have

$$Z = (1 - j) \sqrt{\frac{R}{2\omega C}} \coth (1 + j) \sqrt{\frac{\omega RC}{2}} \tag{87}$$

or

$$Y = (1 + j) \sqrt{\frac{\omega C}{2R}} \tanh (1 + j) \sqrt{\frac{\omega RC}{2}} \qquad (88)$$

Hyperbolic functions of 45 deg arguments are tabulated in Ref. 8. The input impedance is plotted in Fig. 37 for reference.

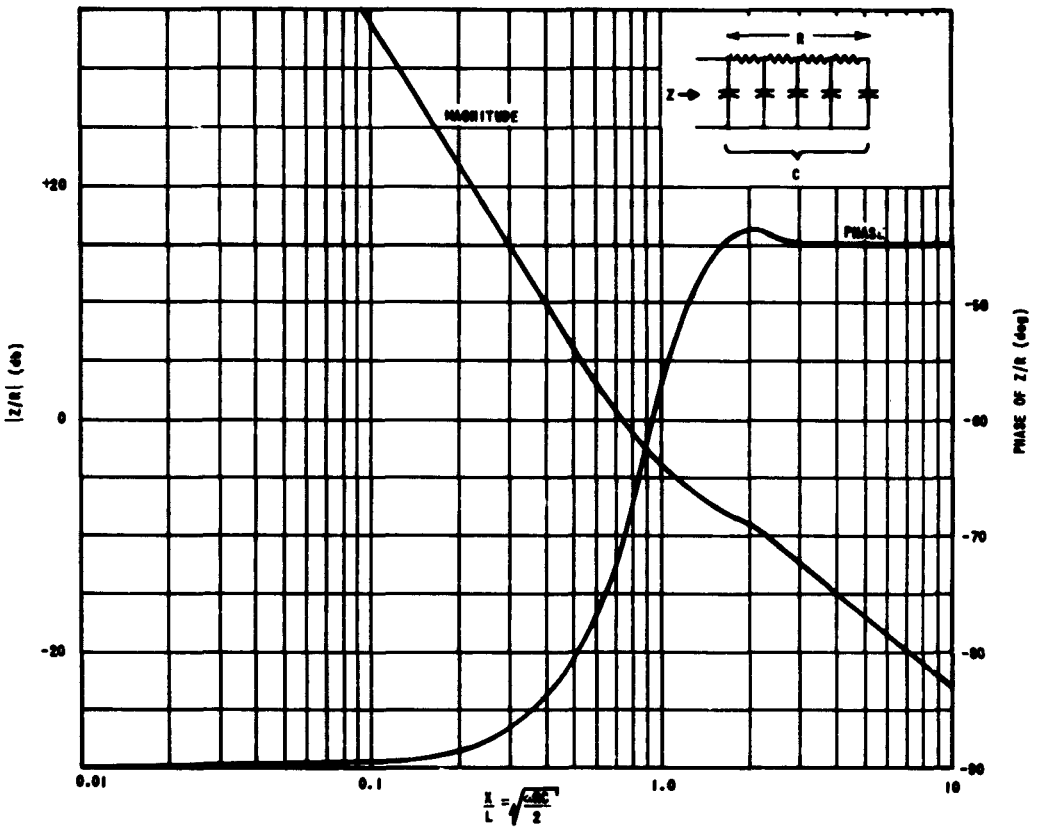


FIG. 37. MAGNITUDE AND PHASE OF THE INPUT IMPEDANCE OF AN OPEN-END RC TRANSMISSION LINE.

It is informative to plot (82) vs x for various $X/L = \sqrt{\omega RC/2}$ as shown in Fig. 38. The plots represent that portion of the voltage applied to the line that reaches various parts of the line. Suppose we

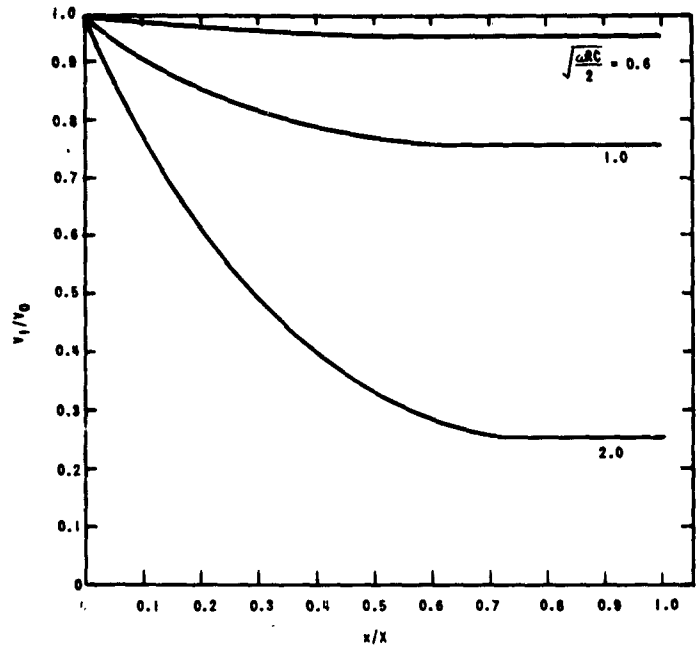


FIG. 38. VOLTAGE VS DISTANCE ALONG AN OPEN-END RC TRANSMISSION LINE.

consider again the case where the voltage applied to the base does not cause significant conduction. Then we can use Fig. 38 to visualize the voltage across the emitter junction with respect to that at the emitter edge by setting $R = R_{BI}$ and $C = C_E + C_{CI}$ and calculating $\sqrt{\omega RC/2}$ for the frequency we are considering. The resulting distribution of voltage along the line sets a lower limit on the current crowding. If the drive were then increased there would be more crowding due to conduction.

When we consider that V_o = 1 to 4 v peak and the emission current density will vary as

$$\exp\left[\frac{q(V_1 - V_{BB})}{n\,kT}\right] \simeq \exp\left(\frac{V_1 - V_{BB}}{0.05}\right)$$

then it is apparent that a rather small variation in voltage evident from Fig. 38 will result in very crowded emission. If we arbitrarily select

$$\sqrt{\frac{\omega R_{BI}(C_E + C_{CI})}{2}} = 1$$

as that condition which divides crowded and noncrowded operation for nonconduction drive, we can obtain a line cutoff frequency

$$F_L \triangleq \frac{1}{\pi R_{BI}(C_E + C_{CI})} \tag{89}$$

above which only the emitter edge is effective even at the lowest collector current levels. For the 2N1506 transistor, measurements to be described later gave $R_{BI} = 105\Omega$. $C_E = 81$ pf at $V_{BB} = 2.5$ v, and $C_{CI} = 2.77$ pf at $V_{CC} = 40$ v. From these values

$$F_L = 27.6 \text{ Mc} \qquad (2N1506)$$

When we try to apply this concept to a transistor such as the TA2084, it becomes a little difficult to decide what values R_{BI} and C_E should have. This calculation is performed in Appendix C. The result is

$$F_L = 268 \text{ Mc} \qquad (TA2084)$$

The input power to the RC line can also be obtained in closed form from

$$P = \frac{1}{2} \text{Re } I(0)\,\overline{V(0)}$$

$$= \frac{1}{2} \text{Re } \frac{V_0^2}{RL}\left[\frac{\cos\frac{X}{L}\sinh\frac{X}{L} - \sin\frac{X}{L}\cosh\frac{X}{L} + j\left(\sin\frac{X}{L}\cosh\frac{X}{L} + \cos\frac{X}{L}\sinh\frac{X}{L}\right)}{\cos\frac{X}{L}\cosh\frac{X}{L} + j\sin\frac{X}{L}\sinh\frac{X}{L}}\right] \tag{90}$$

After some simplification this becomes

$$\frac{P}{V_0^2/R} = \frac{1}{2}\sqrt{\frac{\omega RC}{2}}\left[\frac{\sinh\sqrt{\frac{\omega RC}{2}}\cosh\sqrt{\frac{\omega RC}{2}} - \sin\sqrt{\frac{\omega RC}{2}}\cos\sqrt{\frac{\omega RC}{2}}}{\sinh^2\sqrt{\frac{\omega RC}{2}} + \cos^2\sqrt{\frac{\omega RC}{2}}}\right] \qquad (91)$$

where the power has been normalized so that it is a function of $X/L = \sqrt{\omega RC/2}$. The normalized power is plotted in Fig. 39 along with

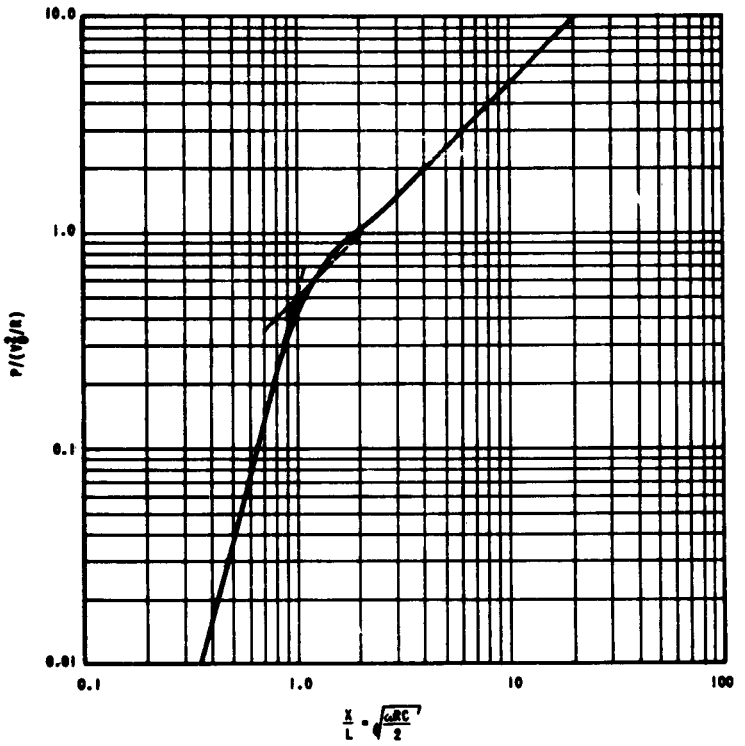


FIG. 39. NORMALIZED INPUT POWER TO AN RC TRANSMISSION LINE.

the extended asympotes. These are seen to intersect very near $\sqrt{\omega RC/2} = 1$ which we had previously selected to define the line cutoff frequency. The asymptotic forms of (91) are also useful. They are,

$$P \simeq \frac{V_0^2}{2R} \sqrt{\frac{\omega RC}{2}} \text{ for } \sqrt{\frac{\omega RC}{2}} > 4.0 \qquad (92)$$

$$P \simeq \frac{V_0^2}{6} R\,(\omega C)^2 \text{ for } \sqrt{\frac{\omega RC}{2}} < 0.25 \qquad (93)$$

Figure 39 indicates that the error would not be over 25 percent if (92) were used for $\sqrt{\omega RC/2} > 1$ and if (93) were used for $\sqrt{\omega RC/2} < 1$.

Equations (91) - (93) and (87) enable us to obtain an approximation to the input ac power due to junction charging. The main question is, "With what transistor parameters do R and C in these equations correspond?" For frequencies low compared to F_L, it is nearly true that the entire line charges to the same voltage with the same phase everywhere. In this case the collector capacitance C_{CI} acts just like a Miller effect capacitance so that the total shunt capacitance should be

$$C = C_E + \left(1 + \frac{V_{CC} - V_{C,min}}{V_0}\right) C_{CI} \qquad (94)$$

For frequencies high compared with F_L, only the first part of the line is effective in causing emission and here the phase of the line voltage has not changed much from the applied phase. Again the same value for total C should be used. These assumptions imply that the collector voltage is 180 deg out of phase with the base voltage. As has previously been pointed out, this is not exactly true since the collector voltage may actually lag by an additional 30 to 50 deg. Because the effect of C_{CI} is small compared to C_E, the additional lag has been ignored here. The appropriate value for R is $R = R_{BI}$. One possibility for choosing C_E and C_{CI} would be to take the average value over the swing of junction voltages which will occur. This choice does not seem to be warranted, however, so that C_E and C_{CI} will be taken as their small-signal values at the bias points.

With the value of C given by (94), a different line cutoff frequency results. The designation F_L will be retained for the case of $V_{C,min} \simeq V_{CC}$ and f_L will be used for the general case.

$$f_L \triangleq \frac{1}{\pi R_{BI}\left[C_E + \left(1 + \frac{V_{CC} - V_{C,min}}{V_O}\right)C_{CI}\right]} \tag{95}$$

As an example, the input ac power due to junction charging has been calculated for the 2N1506 transistor and is shown in Fig. 40 for V_{CC} = 40 v and for two values of V_{BB}, 0 and 2.5 v. The procedure was to

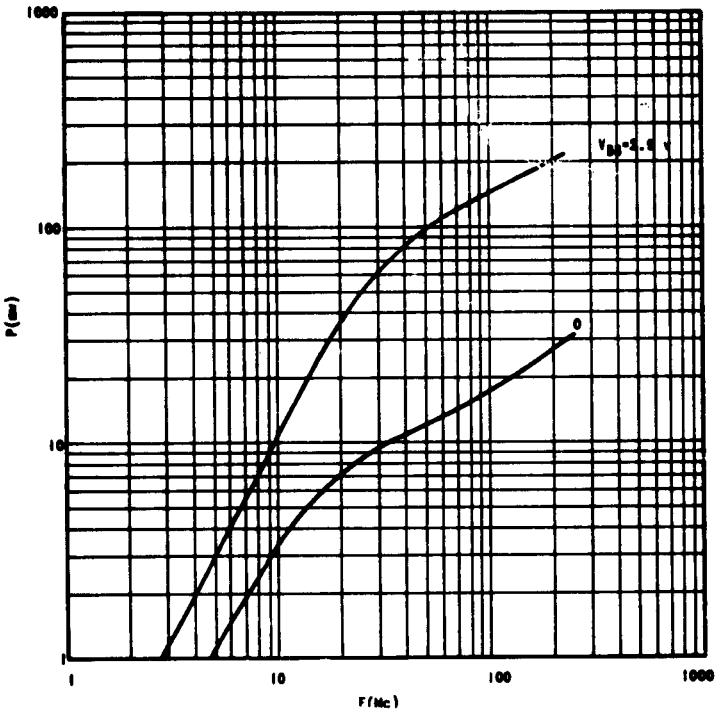


FIG. 40. JUNCTION CHARGING LOSSES FOR THE 2N1506 TRANSISTOR, V_{CC} = 40 v.

assume that at each frequency the drive was adjusted so that the peak voltage at the line was 1.0 v (cf Fig. 41). This is a median value for the range of collector currents in which we are interested. The peak ac voltage at the line input is then $V_{BB} + 1.0 = V_O$. Using $|Z|$ from Fig. 37 the peak input current is

$$I_O = \frac{V_C}{|Z|} \tag{96}$$

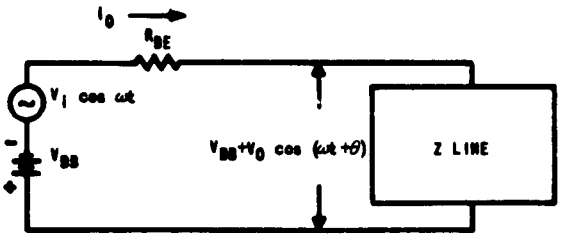


FIG. 41. EQUIVALENT CIRCUIT FOR JUNCTION CHARGING LOSSES.

The power lost in R_{BE} is

$$P_{R_{BE}} = \frac{1}{2} I_0^2 R_{BE} = \frac{V_0^2}{2|Z|^2} R_{BE} \tag{97}$$

The power lost in the line is found from Fig. 39 and this is added to $P_{R_{BE}}$ to give the total input ac power due to junction charging.

2. Measurement of Line Parameters

Emitter and collector depletion capacitances may conveniently be measured as functions of applied dc voltage using a small signal impedance bridge. If the collector lead is left open and measurements are made between base and emitter leads at a low enough frequency, the RC line will be effectively short and only C_E will be obtained. Similarly one may leave the emitter lead open and measure between base and collector to obtain $C_{CI} + C_{CE}$. The frequency chosen must be low enough so that the line is purely capacitive. For a 5 percent error in the capacitance measurement, the frequency should be

$$f \leq \frac{1}{2\pi R_{BI} (C_E + C_{CI})} \tag{98}$$

and

$$f \leq \frac{1}{6\pi R_{BE} (C_E + C_{CI})} \tag{99}$$

In the case of the 2N1506 transistor this requires that $f \leq 10$ Mc.

If the geometry of the transistor is known, C_{CI} and C_{CE} may be obtained by calculation from the measured sum $(C_{CE} + C_{CI})$ and from

$$\frac{C_{CI}}{C_{CE}} = \frac{A_E}{A_B - A_E} \tag{100}$$

where A_E = emitter-base junction area and A_B = collector-base junction area. A novel method which does not depend on knowing the geometry uses C_E and C_{CI}. This method has been found useful in cases where C_E/C_{CI} is not too large (150:1 or less). The circuit used is that of Fig. 42.

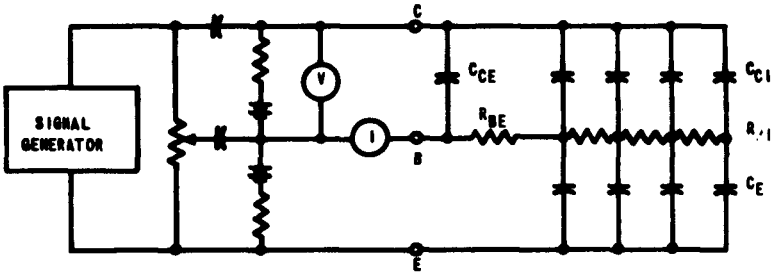


FIG. 42. CIRCUIT FOR MEASUREMENT OF C_{CE} AND C_{CI}.

The basis for the measurement is that C_{CI} and C_E form a capacitive voltage divider and if the potentiometer is set to the same ratio there is no voltage across R_{BE} or R_{BI}. The potentiometer is set for (V) and (I), the voltage and current oscilloscope probes, to be 90 deg out of phase indicating only capacitive current, i.e., no current through R_{BE}, the balance condition. C_{CE} is then obtained from measuring (V) and (I) and knowing the frequency. This same circuit may then be used to measure $C_{CE} + C_{CI}$ by turning the potentiometer to the bottom and reading (V) and (I) with E disconnected. Next, the potentiometer can be turned to the top and C disconnected to read (I) to give C_E in the same way. For the last two readings the frequency must be low as given in (98) - (99). For the balance condition, however, the frequency

is not critical and in fact the higher it is the more sensitive will be the current reading and the more rapidly will the relative phase of (V) and (I) change as the adjustment is made.

Using this technique to measure C_{CI} and C_{CE} for the 2N1506 transistor at $V_{CE} = 10$ v, $V_{ER} = 5$ v, gave

$$C_{CI} = 4.7 \text{ pf}, \qquad C_{CE} = 13.8 \text{ pf}$$

Using bridge measurements of C_C and the ratio of areas give

$$C_{CI} = 4.3 \text{ pf}, \qquad C_{CE} = 11.6 \text{ pf}$$

Internal and external base resistances may be obtained by measuring the impedance between base and emitter with the collector open at a number of frequencies. It is convenient to do this with a bridge which gives the series resistive and reactive components. If the frequency range is limited to a region where the reactance of C_{CE} is large compared to R_{BE}, then the unknown seen by the bridge is R_{BE} in series with an RC trnasmission line as in Fig. 40. At low frequency the series-resistance component of an open RC line is R/3. (This can be shown by taking the real part of Eq. (87) and substituting power series for the various functions involved.) Therefore, the series-resistive component at low frequencies approaches $R_{BE} + \frac{1}{3} R_{BI}$. As the frequency increases, the phase of the line impedance approaches 45 deg and the magnitude of the line impedance approaches zero, leaving only R_{BE}. If other effects such as lead inductance do not become important, it is only necessary to carry the measurements to a frequency where a 45-deg slope has been established for the locus on the impedance plane. Projection of the 45-deg slope to the real axis gives R_{BE}.

An example of this measurement applied to the 2N1506 transistor is given in Fig. 43. R_{BI} and R_{BE} were determined from these data as 105 and 6 ohms, respectively. Using these values and $C_E = 137$ pf from other measurements, the impedance which would be expected from the model was also plotted. The representation is good up to a frequency of several times the line cutoff frequency, indicating that the model is probably acceptable over most of the frequency range. One obvious source of error

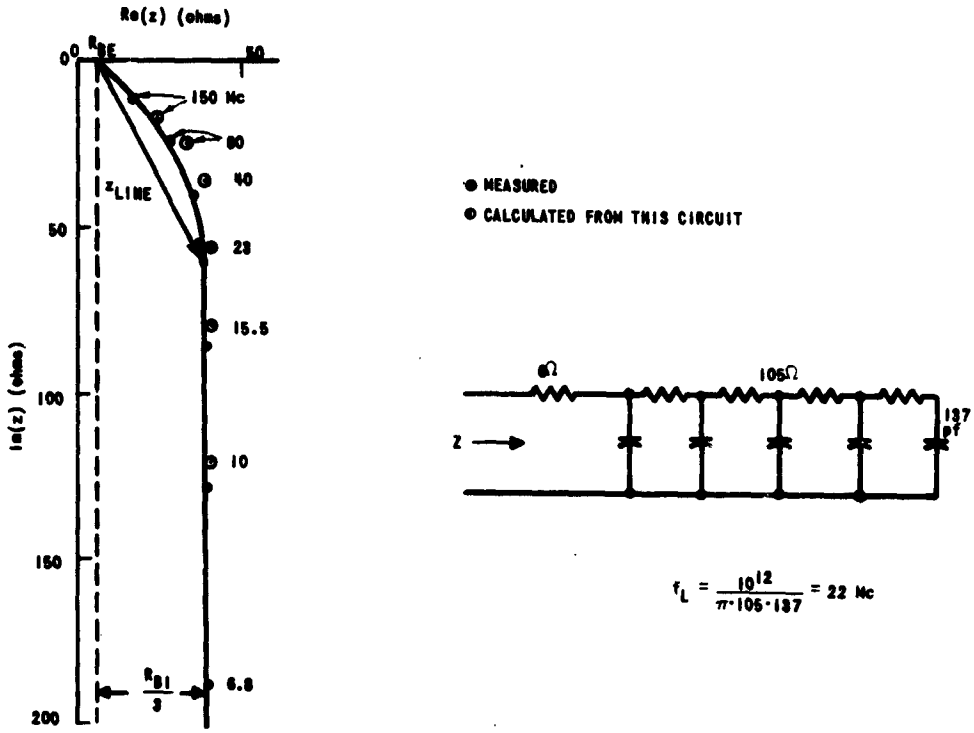


FIG. 43. OPEN COLLECTOR EMITTER-BASE IMPEDANCE FOR THE 2N1506 TRANSISTOR, $V_{BB} = 0$.

is the lead inductance which may amount to 10^{-8} h and if so, would series resonate with the line at somewhere around 150 Mc.

When this measurement technique was applied to the TA2084 Transistor, a different interpretation was necessary, primarily because the much larger capacitance resonated with the lead inductance at an even lower frequency. In this case the impedance actually became inductive at 120 Mc, before a 45-deg slope was established. The real part of the impedance which is approached at high frequency still represents R_{BE} and the real part at low frequency is still $R_{BE} + 1/3\ R_{BI}$ so that the same measurement of impedance at various frequencies still gives the desired information, although it must be handled differently.

3. Base Charging Current Losses

When the diffusion model of a transistor is considered, the base charge is related to the collector current by

$$i_C = \frac{Q_B}{T_C} \tag{101}$$

where T_C is a constant equal to $1/\omega_\alpha$ as long as the transistor is not saturated. For operation in saturation, T_C becomes larger. If recombination, junction charging, and emitter inefficiency currents are neglected in comparison to the charge current flowing in and out of the base, then

$$i_B = \frac{dQ_B}{dt} = T_C \frac{di_C}{dt} \tag{102}$$

This indicates the form of the base charging current. In Fig. 44 are

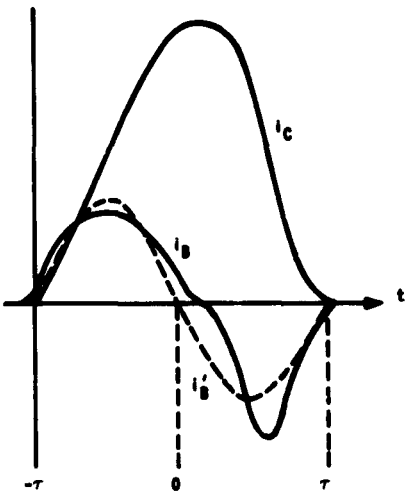


FIG. 44. TYPICAL COLLECTOR CURRENT PULSE i_C; ITS DERIVATIVE, BASE CHARGING CURRENT, i_B; AND A PROPOSED BASE-CHARGING-CURRENT APPROXIMATION i'_B.

shown a typical collector current pulse taken at 18 Mc; its derivative, which is i_B; and a proposed approximation i'_B to the base charging current. The approximation is simply a sine wave beginning and ending when the collector current does, and having an amplitude such that the

integral over a half cycle equals $T_C I_{C,max}$, i.e., the peak charge stored in the base. Letting M equal the peak amplitude of i'_B, M is found as follows:

$$T_C I_{C,max} = \int_0^\tau M \sin \frac{\pi t}{\tau} \, dt \tag{103}$$

$$T_C I_{C,max} = \frac{2M}{\pi\omega} (\omega\tau) = \frac{M}{\pi^2 f} (\omega\tau) \tag{104}$$

$$M = T_C \pi^2 f \frac{I_{C,max}}{(\omega\tau)} \tag{105}$$

The amplitude is seen to vary directly as the frequency and the peak collector current, and inversely as the flow angle. At very low frequencies and low current levels this charge is distributed nearly evenly along the base. However, at large current levels or high frequencies, current crowding causes it to be concentrated near the edge. This crowding is much more severe than the junction charging currents considered previously. In fact the assumption will be made that the base charging current flows only through R_{BE} when power loss is considered. This assumption will neglect power lost in R_{BI} but it may compensate for the incorrect procedure of adding powers in R_{BE} due to two components of current, base charging and junction charging. Under these assumptions the energy lost in R_{BE} per cycle is

$$E = R_{BE} \int_{-\tau}^{\tau} \left(T_C \pi^2 f \frac{I_{C,max}}{\omega\tau} \right)^2 \sin^2 \frac{\pi t}{\tau} \, dt \tag{106}$$

$$= R_{BE} \left(T_C \pi^2 f \frac{I_{C,max}}{\omega\tau} \right)^2 \tau \tag{107}$$

The power is fE,

$$P = \frac{R_{BE} T_C^2 \pi^3}{2} f^2 \frac{(I_{C,max})^2}{(\omega\tau)} \tag{108}$$

As an example, the 2N1506 transistor has $R_{BE} = 6\Omega$ and $T_C = 1.06 \times 10^{-9}$ ($f_\alpha = 150$ Mc). If $I_{C,max} = 0.5$ amp and $\omega\tau = 1$ radian, then at various

frequencies the following base charging power would be required:

f (Mc)	P (mw)
1	0.026
10	2.6
100	260

The base charging power calculated in this way is most accurate where the assumption of current flow only through R_{BE} is reasonable, i.e., at the higher frequencies. At 1 Mc, for example, the result may be significantly low.

In summary, three sources of input ac power have been derived and calculated for specific examples using the 2N1506 transistor. The recombination loss is on the order of 0.1 mw to 1 mw and does not vary with frequency. The junction and base charging losses are on the order of 0.05 to 0.5 mw at 1 Mc. At 10 Mc the junction charging power is 5 to 10 mw while the base charging power is about 3 mw. At 100 Mc the junction charging power is 50 to 200 mw and the base charging power is 200 to 300 mw. The dominant source of power loss changes from recombination at quite low frequency to junction and base charging at medium and high frequency.

D. TESTS OF A VHF CLASS C AMPLIFIER

A 2N1506 transistor was operated in the 45-Mc amplifier circuit of Fig. 45. The tests were somewhat limited because of test equipment capability. The drive power available was about 100 mw, which was not enough when operating with much reverse base bias. A sampling oscilloscope was used but no commercial current probe was available for this frequency. A probe was made from a ferrite toroid. Its phase and amplitude response appeared satisfactory based on dual-trace measurements of the voltage across a known resistance and on the current indicated by the probe through the resistance. However, it is not known what effect other properties (shielding, balance, additional inductance introduced into the circuit, etc) may have had on the measurements.

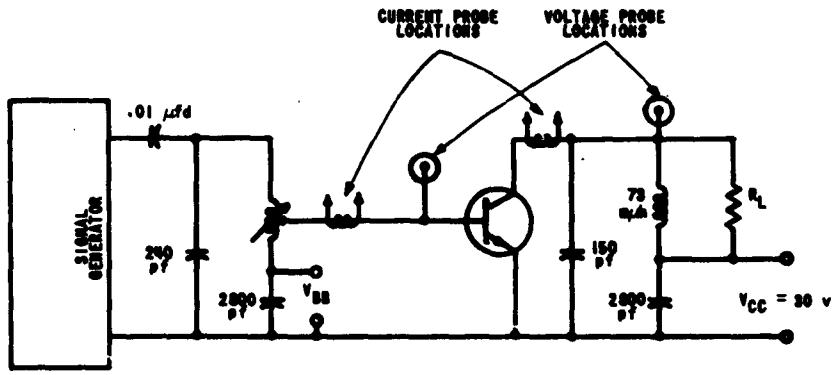


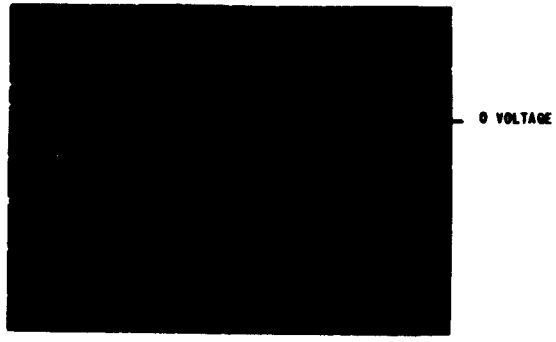
FIG. 45. VHF CLASS C AMPLIFIER.

The circuit was tuned by adjusting the frequency of the signal generator and tuning the input tank. Load power was measured by observing the collector voltage and knowing the load resistance. The criterion for optimum tuning was maximum collector efficiency.

Waveforms from the circuit are shown in Fig. 46. Several interesting facts are apparent.

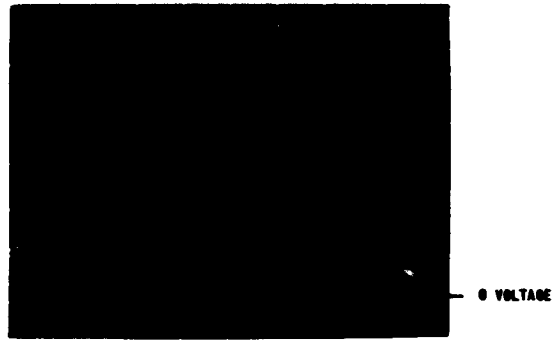
1. The base current waveform is largely sinusoidal rather than pulse like, indicating that a large portion of the current is due to junction charging as anticipated.
2. The base and collector voltages are now out of phase by almost a full cycle. Three factors appear to cause the additional lag. R_{BE} in series with the RC line causes the voltage at the line to lag V_B by an additional 15-20 deg at this frequency. The base transit time amounts to another 15-20 deg at this frequency. These factors together with current stretching account for the lag of V_C with respect to V_B.
3. The collector current now contains a large proportion of junction charging current, so much so that the pulse is somewhat obscured.
4. The collector current pulse does not appear to occur at the collector voltage minimum. No good explanation is available for this.

Because of an accident to the first 2N1506 transistor, the 2N1506 used in this test was a new unit. To calculate the expected performance it was necessary to make the open-collector, emitter-base impedance measurements again and to obtain f_α from β and f_β measurements.



a. Base voltage (1 v/cm)
Base current (70 ma/cm)

b. Base voltage (1 v/cm)
Collector voltage (10 v/cm)



c. Collector current (140 ma/cm)
Collector voltage (10 v/cm)

FIG. 46. WAVEFORMS OF 45-Mc AMPLIFIER (2N1506 Transistor with V_{CC} = 30 v, V_{BB} = 0, R_L = 192Ω).

These gave values of $R_{BE} = 6.5\Omega$, $R_{BI} = 16\Omega$, $C_E = 177$ pf at 0 v, and $f_\alpha = 115$ Mc. Except for R_{BE} these values are considerably different from those for the first 2N1506, and it appears that the emitter diffusion did not penetrate as deeply. This difference would give a larger base width resulting in decreased f_α and decreased R_{BI}. The larger C_E would result from higher base doping which would exist at the emitter side of the base.

Measured and predicted performances are given in Table 7. For all tests, $V_{CC} = 30$ v, f = 45 Mc.

TABLE 7. RESULTS OF 45-MC AMPLIFIER FOR THE 2N1506 TRANSISTOR

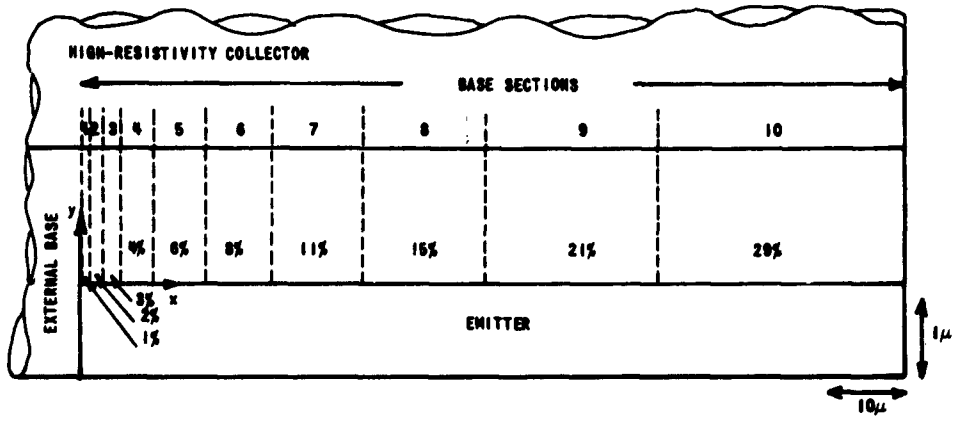
Operating Condition					Measured			Predicted		
V_{BB} (v)	R_L (ohm)	$I_{C,max}$ (ma)	$\omega\tau$ (deg)	$V_{C,min}$ (v)	P_L (w)	E_C (%)	$P_{in,ac}$ (mw)	P_L (w)	E_C (%)	$P_{in,ac}$ (mw)
0	192	230	81	7	1.38	70	67	1.26	63	31
-0.4	192	260	73	7	1.38	73	113	1.33	65	53
-0.4	324	190	70	4	1.08	78	105	1.07	75	44

The load power P_L was calculated using Eq. (10), and the efficiency E_C was calculated using Eq. (11). Although these are the results of the simplest analysis it is doubtful if a more detailed analysis is warranted at this stage. The input ac power was calculated using the sum of junction charging and base charging power from Eq. (97) and (108) and Fig. 39. The agreement in load power and efficiency is quite good considering all things. The predicted ac input power shows the right trend in approximately the right proportion but is only about half as large as it should be. This is probably due to neglecting saturation. For these cases, some part of the collector junction is almost surely forward biased so that the base charging current was larger than for a nonsaturated case and penetrated deeper into the base, thus resulting in more loss.

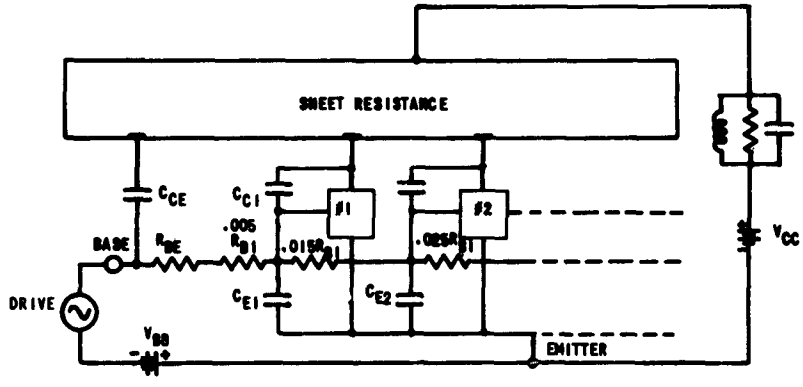
VI. ANALOG SIMULATION OF A VHF POWER TRANSISTOR

A. INTRODUCTION

Because the exact solution of the two-dimensional, nonlinear, time-varying problem by analytic means is not reasonable, an analog which could give the solution to specific operating conditions was sought. Beale and Beer [Ref. 1] have performed an analog simulation which took two-dimensional effects into consideration while simulating operation at 100 Mc. The equivalent circuit on which their simulation was based was the hybrid pi. No provisions were made for simulating collector saturation so that a very important element was neglected. The method of simulation to be described here is based on the Linvill two-lump excess charge density model [Ref. 2]. In order to take account of the lateral variations of current and voltage in the base, a number of two-lump models can be used. For simplicity, the 2N1506 transistor was chosen to be simulated since its long emitter stripe configuration is simply represented by the open-ended RC line. Any transistor geometry which can be reduced to this case at the frequency to be studied can be represented in this way. At very high frequencies all geometries result in operation only at the emitter edge so that for the most important area to be studied, this same approach is suitable. Since the construction is symmetrical about a vertical plane through the center of the emitter, no current flows across this plane, and it can be considered to be the open end of the line. The length of the open-end transistor is then twice the emitter length in the actual transistor. The length is assumed long enough so that current flow occurs only in cross-sectional planes. The base may be broken up into a number of sections as indicated in the cross-sectional view in Fig. 47a, and each section may be represented by a two-lump model. The widths of the sections should be chosen to be narrow under the emitter edge and wider toward the end of the line, so that each section carries approximately the same current. (An x-y coordinate system is also defined in Fig. 47a.) Since the 2N1506 is similar to the transistor simulated by Beale and Beer, the widths suggested in Fig. 47a were based on the distribution of current density found in their study. Ten sections are shown with widths of 1, 2, 3,



a. Transistor cross section



b. System connections

FIG. 47. SIMULATION OF THE 2N1506 TRANSISTOR.

4, 6, 8, 11, 15, 21, and 29 percent of the emitter width. The following assumptions were made:

1. The emitter is an equipotential region because of its high doping.
2. Lateral (x) current flow in the base is by drift of majority carriers. The base sheet resistivity is constant.
3. Flow from emitter to collector is by diffusion only.
4. The base thickness and collector thickness are not functions of collector voltage and the collector is all the same resistivity. The n+ collector is an equipotential region.
5. Emitter-collector diffusion current fringing into the external base is not significant.
6. A constant depletion capacitance is a satisfactory approximation.
7. The emission efficiencies of the junctions are constant.

Based on these assumptions the system shown in Fig. 47b will simulate the transistor. The collector is simulated by a sheet of resistance paper having the same relative dimensions as the n+ collector cross section. The circuits which simulate the base sections are connected to the resistance paper with the same relative geometry as the base sections being simulated. The base sheet resistance becomes a series of resistors with values proportional to the section widths to which the base leads of the base circuits are connected, and the emitter leads are connected together. C_{CE} and R_{BE} are each lumped in one component. C_{CI} and C_E are lumped in proportion to the section width.

B. SIMULATION OF THE TWO-LUMP MODEL

The two-lump model shown in Fig. 48 has been used frequently where both junctions may be either forward or reverse biased since it includes the effects of storage in the base, recombination and emission efficiency, and diffusion. In this model, currents are functions of the excess minority carrier density at the emitter and collector ends of the base. The excess densities are assumed to follow the low-level law of the junction

$$n_e = n_{p1}\left[\exp\left(\frac{qV_{EB}}{nkT}\right) - 1\right] \tag{109}$$

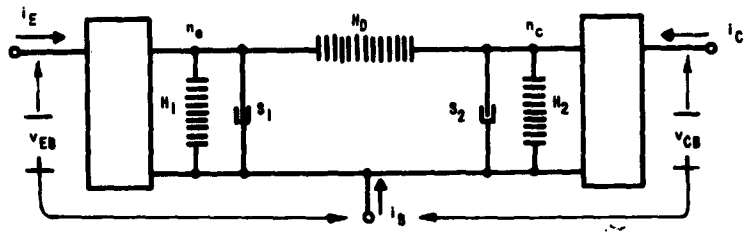


FIG. 48. TWO-LUMP EXCESS-CHARGE-DENSITY MODEL.

$$n_c = n_{p2}\left[\exp\left(\frac{qv_{CB}}{nkT}\right) - 1\right] \tag{110}$$

The base, emitter, and collector currents are obtained as though n_e and n_c were voltages and the H's and S's were conductances and susceptances, to give

$$i_B = H_1 n_e + S_1 \frac{dn_e}{dt} + H_2 n_c + S_2 \frac{dn_c}{dt} \tag{111}$$

$$i_E = H_D(n_c - n_e) - H_1 n_e - S_1 \frac{dn_c}{dt} \tag{112}$$

$$i_C = H_D(n_e - n_c) - H_2 n_c - S_2 \frac{dn_c}{dt} \tag{113}$$

A circuit which acts in an exactly analogous way is shown in Fig. 49. Basically it depends on the use of silicon diodes to establish the same exponential relations which occur in the two-lump model. In the two-lump model, excess charge density is proportional to the voltage according to Eqs. (109) and (110). In the circuit, the resistors R_1 and R_2 are chosen small enough at all currents of interest so that the voltage across the impedance is much smaller than that across the diode. (Actually, $V_{impedance} < nkT/q = 0.045$ v. If this is true, the diode currents follow the usual diode law

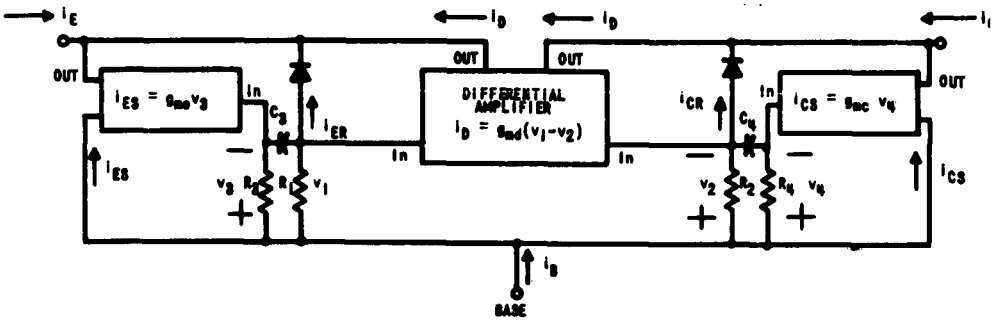


FIG. 49. ANALOG FOR THE TWO-LUMP MODEL.

$$i_{ER} = I_{S1}\left[\exp\left(\frac{qv_{EB}}{nkT}\right) - 1\right] \tag{114}$$

and

$$i_{CR} = I_{S2}\left[\exp\left(\frac{qv_{CB}}{nkT}\right) - 1\right] \tag{115}$$

Therefore, if a diode is chosen which has the same value of n as the transistor, the current is analogous to the excess charge density. Further, if $n_{p1}H_1 = I_{S1}$, the diode current is exactly the combinance current and $i_{ER} = H_1 n_e$.

The small sampling resistors R_1 and R_2 provide an input voltage analogous to the difference of excess carrier densities to a differential amplifier. The amplifier has high output and input impedance so that it acts as a voltage input - current output amplifier to form the diffusion current.

Resistor-capacitor differentiators where $R_3 \gg R_1$ and $R_4 \gg R_2$ provide voltages to amplifiers with high output impedances to form the storance currents. The voltages at the inputs to the storance amplifiers are approximately

$$v_3 = R_1 R_3 C_3 \frac{di_{ER}}{dt}; \qquad v_4 = R_2 R_4 C_4 \frac{di_{CR}}{dt} \tag{116}$$

as long as the frequency is low compared to $1/(2\pi R_2 C_2)$ and $1/(2\pi R_4 C_4)$. Since the current is analogous to the excess charge density, applying this voltage to a high-impedance amplifier forms a current equal to the storance current.

The equations for the terminal currents of the circuit are

$$i_B = i_{ER} + i_{ES} + i_{CR} + i_{CS} = i_{ER} + g_{me} R_1 R_3 C_3 \frac{di_{ER}}{dt} + i_{CR} + g_{mc} R_2 R_4 C_4 \frac{di_{CR}}{dt} \tag{117}$$

$$i_E = -i_{ER} - i_{ES} - i_D = g_{md}(R_2 i_{CR} - R_1 i_{ER}) - i_{ER} - g_{me} R_1 R_3 C_3 \frac{di_{ER}}{dt} \tag{118}$$

$$i_C = i_D - i_{CR} - i_{CS} = g_{md}(R_1 i_{ER} - R_2 i_{CR}) - i_{CR} - g_{mc} R_2 R_4 C_4 \frac{di_{CR}}{dt} \tag{119}$$

These are seen to be the same as Eqs. (111), (112), and (113) if

$$\left.\begin{aligned} I_{S1} &= n_{p1} H_1 \\ I_{S2} &= n_{p2} H_2 \\ g_{me} R_1 R_3 C_3 &= S_1/H_1 \\ g_{mc} R_2 R_4 C_4 &= S_2/H_2 \\ R_1/R_2 &= H_2/H_1 \\ \text{and} \\ g_{md} R_1 &= H_d/H_1 \end{aligned}\right\} \tag{110}$$

If these conditions are satisfied, the analogy will be exact. As usual, however, practical considerations result in some additional complications. In the first place, one of the objectives of making a simulation of a vhf power transistor is to enable the simulator to operate at lower current levels and lower frequencies. Lower current levels allow the simulator to use components in their low-current, high-linearity, low-power dissipation range. Lower frequency operation allows the use of audio-frequency components, removes interconnecting lead-inductance

problems, and allows observation of waveforms and other measurements to be made with simple test equipment.

The use of current scaling, together with the fact that the base is broken up into some very small sections, means that finding a diode where $I_S = n_p H$ for a current-scaled section is impossible. Diode junction areas are just not that small. As an example, the first section of a 2N1506 simulation would represent only 1 percent of the base, whereas a current scaling of 56:1 is desirable for the resistance paper available and the current capabilities of the active components available. Therefore, a diode current 1/5600 times that of the base current of the 2N1506 transistor would be required. This would be (1/5600) x 50 ma at 1.37 v, requiring $I_S = 0.56 \times 10^{-12}$ μamp.

What is desired, however, is not an exact simulation over all ranges but a close approximation over the normal operating current range (scaled). This approximation is achieved by adding a small reverse-bias voltage as indicated in Fig. 50. This is adjusted so that the correct diode current

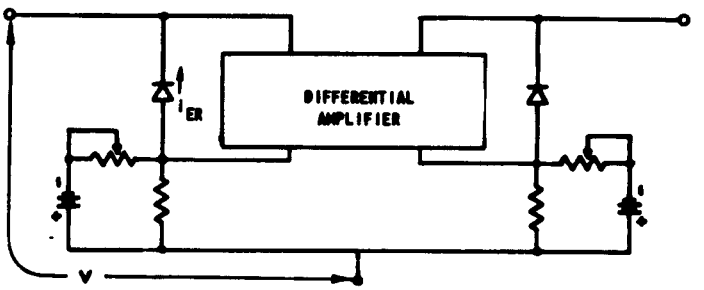


FIG. 50. PARTIAL ANALOG CIRCUIT SHOWING REVERSE BIASING OF DIODES.

will flow at some point in the normal operating range. The terminal voltage V is related to the current i_{ER} by

$$i_{ER} = I_{sat} \left\{ \exp\left[\frac{q(V - V_{bias})}{nkT}\right] - 1 \right\}$$

$$= I_{sat} \exp\left(\frac{-qV_{bias}}{nkT}\right) \left[\exp\left(\frac{qV}{nkT}\right) - \exp\left(\frac{qV_{bias}}{nkT}\right)\right] \qquad (121)$$

Since significant current flow occurs only when $V > V_{bias}$, the second term in the bracket can be dropped. Likewise the second term in Eq. (120) can be dropped, and the two equations are the same when

$$I_{SI} = I_{sat} \exp\left[-\left(\frac{qV_{bias}}{nkT}\right)\right] \qquad (122)$$

The effective saturation current of the actual diode has thus been much reduced, yet the exponential relations hold well over the useful range.

An example of this is shown in Fig. 51 where the emitter-base characteristics of three different silicon vhf transistors are plotted. It

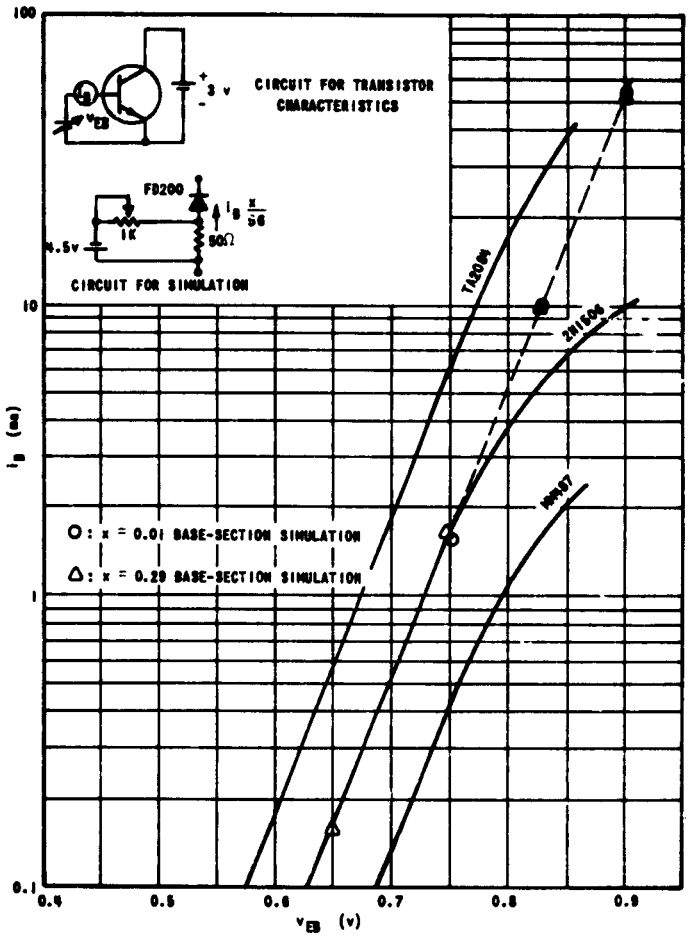


FIG. 51. TRANSISTOR EMITTER-BASE CHARACTERISTICS COMPARED TO THE SIMULATION OF CERTAIN BASE SECTIONS.

is apparent from the slopes at low currents that they all have nearly the same $nkT/q = 0.045$ v. The upper portions of each characteristic bend over because voltage drop in the base resistance is becoming important. Since base resistance is separately accounted for in the analog, a straight-line continuation of the lower portion is what should be simulated. This is shown as a dashed line on the 2N1506 curve. Also shown is the result of biasing an FD200 diode so that it will match a base section at 10 ma total base current. A current scaling of 56:1 and the two extreme base sections, 1 and 29 percent, are shown. Excellent agreement exists over the useful current range.

The bias voltages for the emitter and collector sampling resistors will generally not be the same. The differential amplifier must therefore have enough range in its differential balance control to compensate for this. Other requirements for the differential amplifier are high output impedance, high input impedance, little dc current in the input, good stability, and little capacitive loading or coupling.

The storance amplifiers present the usual problem connected with active differentiation. Because their outputs are returned to their inputs, there is a tendency toward oscillation. The amplifiers must continue to differentiate for several octaves past the frequency of operation because we are dealing with nonlinear operation and the waveforms contain many harmonics. At high frequencies the loop gain must be reduced to unity before the phase lags in the amplifier become 180 deg. This requires some care in amplifier design. In the present case, two of the amplifier stages were chosen to have break frequencies at the high-frequency limit of the RC differentiator and an RC single-phase lead circuit was inserted at a higher frequency to maintain the total phase lag at less than 180 deg until the loop gain became unity.

C. DESCRIPTION OF CIRCUITS DEVELOPED

Because the circuitry required to simulate a two-lump model turned out to be rather formidable, no attempt was made to do a complete two-dimensional simulation. Instead, in order to demonstrate the validity of the idea, a 2N1506 transistor was represented by a single two-lump simulation. The simulated 5-Mc Class C amplifier operating at 10 kc

is shown in Fig. 52, while schematics of the diffusance and storance amplifiers are shown in Figs. 53 and 54.

The storance amplifier is a high-gain linear amplifier with low-frequency response to less than 100 cycles and a high-frequency cutoff of 100 kc. Its input impedance of 500 ohms represents R_3 (Fig. 49) and is large compared to the recombination current sampling resistance (R_1). Together with the differentiating capacitance (C_3), this input impedance provides differentiation to 100 kc, ten times the operating frequency. Q_1 and Q_2 are feedback amplifiers whose gain is determined primarily by the load and feedback resistors. The output stage is rather unusual. It obtains a high output impedance by using a PNP and an NPN transistor collector to collector. The dc operating condition is established by adjusting the 25k potentiometer so that the Q_3 - Q_4 collector voltage is half the supply voltage. Variation of supply voltage then changes the bias condition on Q_3 and Q_4 in exactly the same proportion. The emitter currents therefore change in the same proportion and the collector voltages remain balanced. Measurements have shown that a supply-voltage variation of $\pm$ 30 percent can be tolerated. The ac signal voltage is applied to one transistor, varying its collector current, while the other transistor maintains constant collector current. The difference current flows in the load. The output impedance is quite high because no impedances shunt the collectors of Q_3 and Q_4.

The collector storance amplifier is represented in Fig. 54 except that +90 v is used to power the final stage and 2N698 and 2N1131 transistors are used to handle the larger voltage swing which occurs at the collector.

The diffusance amplifier is a high-gain, linear, differential amplifier. The input voltage is amplified by Q_8 and Q_9. Q_{10} acts as a large impedance in the joint emitter return of Q_8 and Q_9, thus giving a large rejection to common-mode signals at the input. Q_6 and Q_7 further amplify the differential-mode signal and supply additional common-mode rejection. The output stage again makes use of PNP and NPN transistors collector to collector to provide high output impedance. The output stage must remain balanced both as to zero output current for zero input signal and as to collector voltage balance on the output

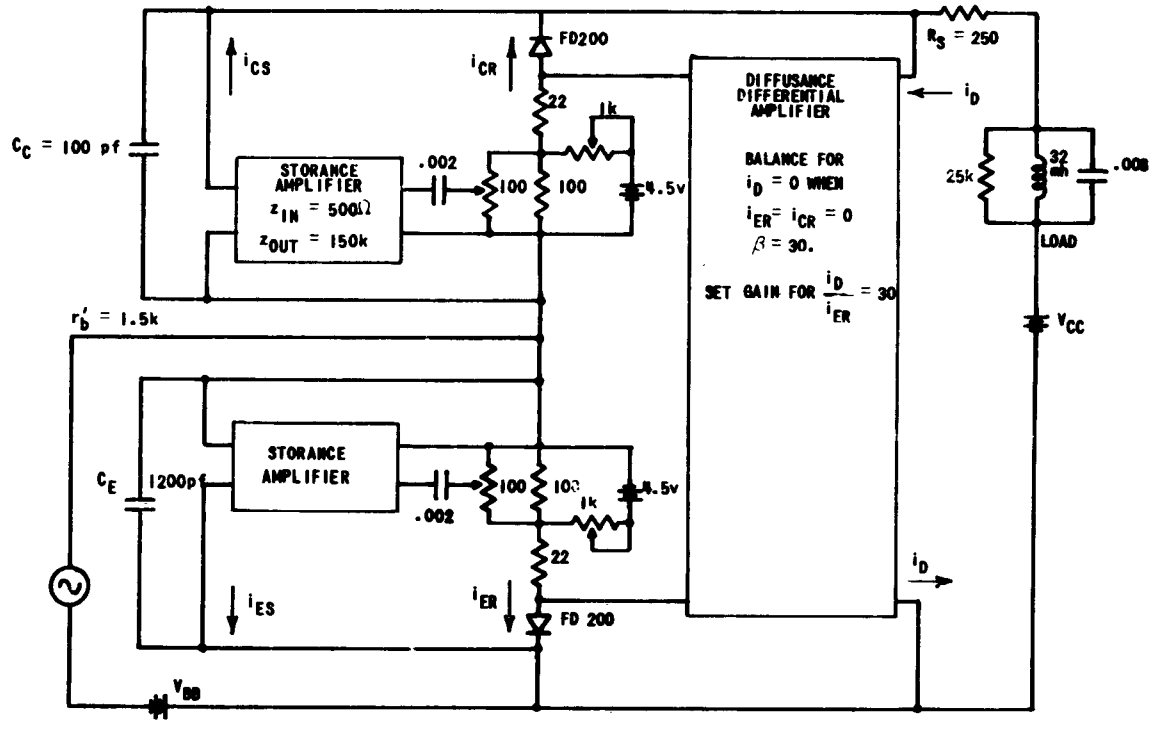


FIG. 52. REPRESENTATION OF A 2N1506 TRANSISTOR BY A SINGLE TWO-LUMP ANALOG SIMULATING A 5-Mc CLASS C AMPLIFIER. Currents scaled down by a factor of 50; frequency down by 500; impedances up by 50, and therefore capacitances up by 10.

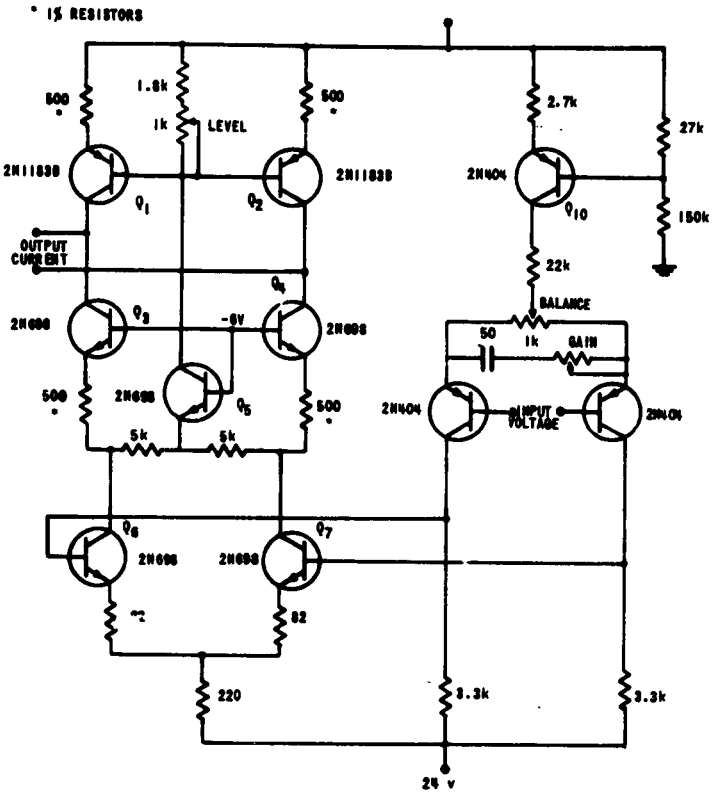


FIG. 53. DIFFUSANCE DIFFERENTIAL AMPLIFIER.

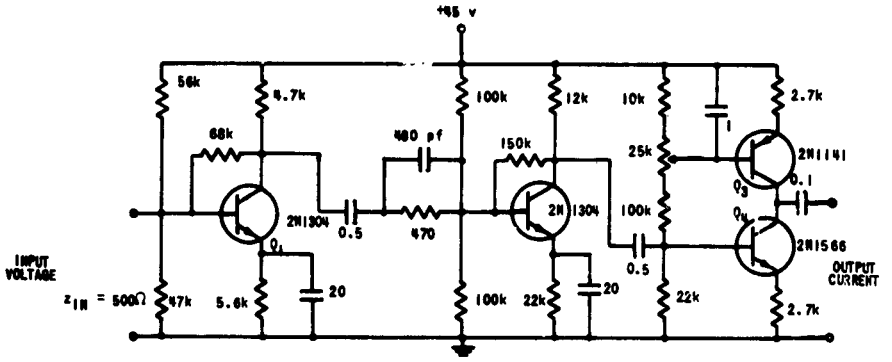


FIG. 54. STORANCE AMPLIFIER.

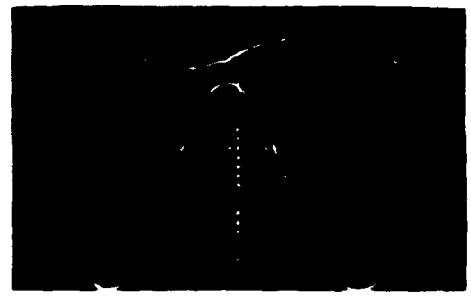
transistors regardless of variation of power supply voltages. This is the function primarily of Q_5. Its emitter current is proportional to the average emitter current of Q_3 and Q_4. The bias voltage applied to Q_1 and Q_2 is derived from the Q_5 collector current. Therefore the Q_1 and Q_2 collector currents are equal and, once set by the level control, remain the same as the average Q_3 and Q_4 current regardless of variation of power supply voltages.

For zero differential input voltage the balance control is used to set the collector voltages of Q_6 and Q_7 equal. This requires the emitter currents of Q_3 and Q_4 to be equal. Adjusting the level control for zero output current then makes the collector currents of Q_1 and Q_2 the same as those of Q_3 and Q_4. Application of a differential voltage at the input, then, causes the currents of Q_3 and Q_4 to change in opposite directions. Since the currents of Q_1 and Q_2 do not change, the difference current flows out through the load and returns.

D. TEST RESULTS

The simulated Class C amplifier of Fig. 52 operates at 10 kc and simulates operation at 5 Mc. The 1.5k value of r_b' corresponds to a 30-ohm base resistance and the 250-ohm vlaue of R_S corresponds to a saturation resistance of 5 ohms. The values of C_C = 100 pf and C_E = 1200 pf correspond to C_C = 10 pf and C_E = 120 pf. The diode biases were adjusted to simulate the 2N1506 emitter-base current-voltage characteristic with 50:1 current reduction. The diffusance amplifier gain was set to give $\beta = 30$ and, finally, the storance amplifier gains were set so that at 10 kc under forward bias small-signal conditions, $i_{ES} = i_{ER}$ and $i_{CS} = i_{CR}$. This simulates forward and reverse f_β = 5 Mc. All of these values are typical of the 2N1506 transistor. The frequency of 5 Mc was chosen as about the highest frequency at which the lateral variations in the base are not too severe and at which a single two-lump model might approximate the actual transistor.

Waveforms from the simulated Class C amplifier are presented in Fig. 55 and may be compared with the waveforms of Fig. 56 which are for



COLLECTOR CURRENT
(2.3 ma/cm)

COLLECTOR VOLTAGE
(10 v/cm)

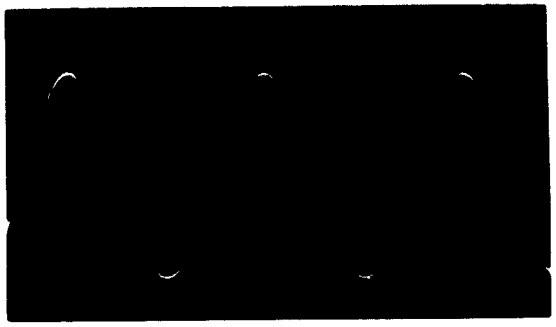
CONDITIONS
V_{CC} = 28 v
V_{BB} = 2.9 v
I_{CDC} = 0.2 ma
R_L = 82 k
P_L = 3.2 mw
$P_{in,dc}$ = 4.6 mw
E_C = 70%

BASE VOLTAGE
(2 v/cm)

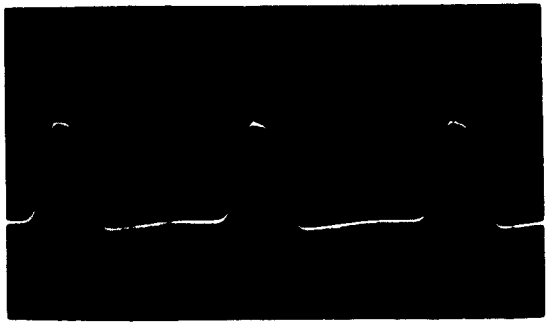
BASE CURRENT
(0.33 ma/cm)

FIG. 55. WAVEFORMS OF A SINGLE TWO-LUMP ANALOG FOR A 2N1506 CLASS C AMPLIFIER OPERATING AT A SIMULATED 5 Mc Drive into saturation.

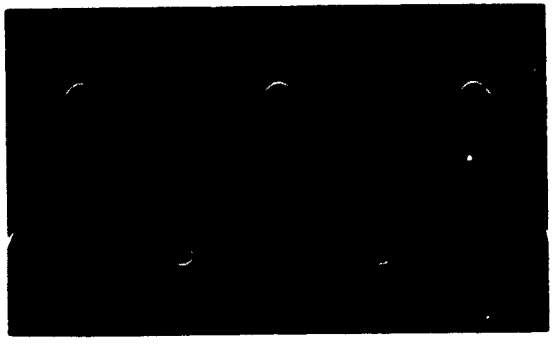
an actual 3-Mc amplifier using the 2N1506 transistor. Except for the fact that the drive in the simulated amplifier has been adjusted to cause saturation, the conditions and the results are quite similar. The base-current waveforms are similar, each showing a basic ac charging current with a superimposed pulse when the transistor conducts. The collector current for the simulated amplifier shows the dip which is characteristic of saturation and indicates that the analog is operating for the moment with the collector junction forward biased. The increased base current in saturation is also evident as a small spike on the base-current waveform.



COLLECTOR VOLTAGE (52 v PEAK TO PEAK)
P_L = 1.48 w



COLLECTOR CURRENT $I_{C,max}$ (0.195 amp)



BASE VOLTAGE (2.1 v PEAK TO PEAK)

BASE CURRENT (10 ma/div)

FIG. 56. WAVEFORMS OF A 2N1506 CLASS C AMPLIFIER OPERATING AT 3 Mc. Drive just to saturation.

Figure 57 presents waveforms from the same simulated 5-Mc amplifier but with the bias voltage decreased to demonstrate operation deep into saturation. In fact, in this case the collector current actually becomes negative during the dip.

Because the analog also has potentially great usefulness in studying switching operation, a set of waveforms showing such operation is presented in Fig. 58. The tuned load was replaced by a 5.6K resistive load, the base bias voltage set to zero, and the base driven by a voltage source pulse generator. Figure 58a shows the case of unsaturated operation. The turn-on transient is rather slow and the turn-off transient begins exactly when the base voltage returns to zero. The reverse base current during turn-off indicates charge being removed from the base. Figure 58b shows the case of saturated operation. A base voltage pulse three times the size of the first case turns the transistor on too rapidly to be recorded with the sweep speed used. When the voltage is returned to zero a storage delay is evident in the collector voltage waveform. Again, reverse base current is noted during turn-off. In recording such transients, the time scaling of 500:1 used in the analog allows the study of very fast transients with low-frequency response equipment.

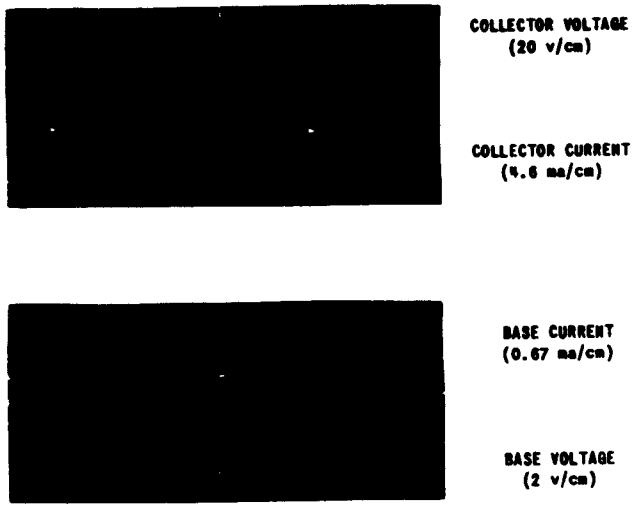
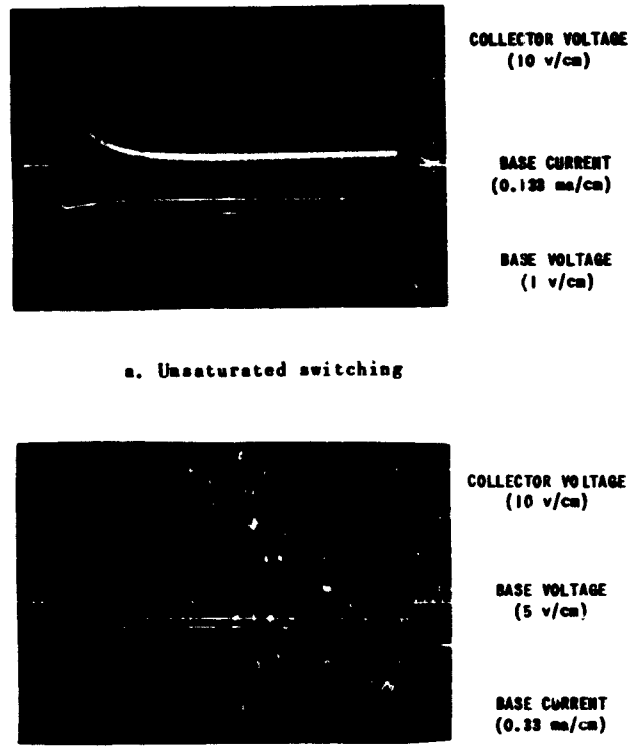


FIG. 57. WAVEFORMS FOR THE SINGLE TWO-LUMP ANALOG FOR A 2N1506 CLASS C AMPLIFIER OPERATING AT A SIMULATED 5 Mc. Same conditions as Fig. 56 except for V_{BB} = 2.5 v to produce deep saturation.



a. Unsaturated switching

b. Saturated switching

FIG. 58. TWO-LUMP ANALOG USED IN SWITCHING OPERATION (V_{CC} = 25 v, V_{BB} = 0, R_L = 5.6K).

VII. CONCLUSION

A. SUMMARY

The operation of power transistors as Class C amplifiers at hf and vhf has been considered from three standpoints:

First, operation at the low-frequency end of the range was studied and both analytic and graphical analyses and design procedures were derived based on approximations to dc collector and base characteristics. These procedures were shown to be reasonably accurate at low frequencies.

Second, operation at intermediate and high frequencies was considered. It was found that emitter current crowding has a great effect on operation. One effect, the apparent increase of transistor saturation resistance, results in operation well into saturation as a common type of high-frequency Class C operation. The decrease of power gain with higher operating frequency was shown to be due primarily to the charging and discharging of the emitter-base and collector-base depletion layers and the base itself through part or all of the base resistance. The RC transmission line formed by the base sheet resistance and the shunt depletion-layer capacitances and base storage capacitance was also shown to limit the narrowness of collector current pulse. This is the primary reason that efficiency decreases at higher frequencies.

Finally, an analog was presented which simulates the two-lump excess-charge-density transistor model. Results of construction and test of a single two-lump approximation of the 2N1506 transistor were presented. The results indicate that if a multiple two-lump model were constructed it could have much usefulness in the study of both Class C operation and switching operation.

B. SUGGESTIONS FOR FURTHER STUDY AND DEVELOPMENT

Some suggestions for possible device improvement are:

1. Mounting of the semiconductor wafer on a thin block of beryllium oxide and internal connection of the emitter contact to the case. This would reduce the emitter lead inductance, allow the case to be mounted directly to the heat sink, and still provide a low thermal resistance path.

2. Mounting as shown in Fig. 59. The proposal is to mount the wafer upside down from the present way. This would reduce the length of the thermal path from 100-150 microns to 2-5 microns because the heat is mainly generated in the collector depletion region near the top of the present arrangement. Mounting on a BeO can bottom would give low thermal resistance. The arrangement could also give very low emitter lead inductance and would simplify mounting and shielding problems. The transistor could be mounted directly in a heat sinking wall. The base and collector leads coming out opposite sides would give minimum stray coupling between input and output.

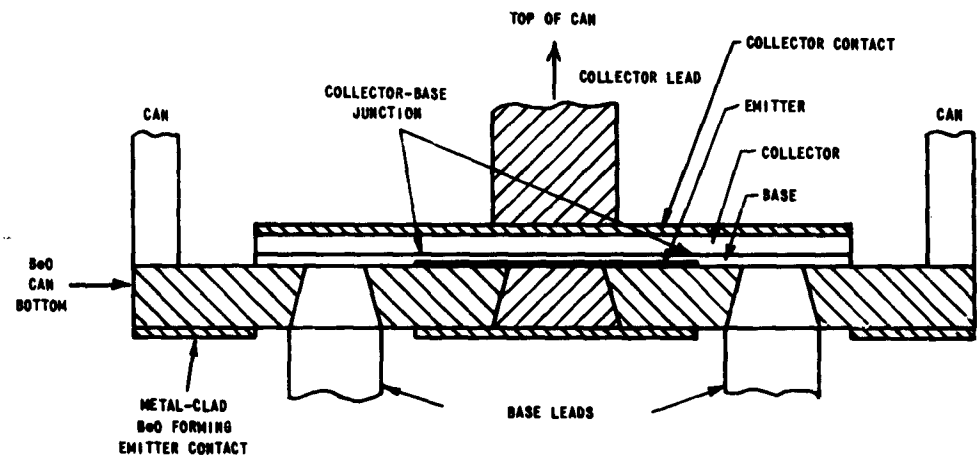


FIG. 59. SUGGESTED MOUNTING ARRANGEMENT.

3. The use of high-resistivity epitaxial layers of such dimensions and doping that the collector depletion region extends across the high-resistivity portion even for very small collector voltages.
4. Continued use of geometries with a ratio of emitter edge to area as high as possible and external base resistance R_{BE} as low as possible so that collector current stretching can be held to a minimum maintaining high efficiency and high power gain to high frequencies.

A further area of suggested study is the construction of a complete two-dimensional analog and its use to study the effect of varying the parameters and geometry of a transistor on its large-signal, high-frequency operation.

APPENDIX A. THE COMPLETE DIFFERENTIAL EQUATION FOR EMITTER-BASE JUNCTION VOLTAGE

The following is a development of a differential equation which is valid in the internal base region under the following assumptions (see Fig. 60):

1. Base conductivity is constant.
2. Minority carrier distribution across the base is linear, i.e., the injected carrier density is enough to overcome any built-in field due to the doping gradient.
3. Majority carrier base current flows as the result of base and junction charging, bulk recombination, and injection inefficiency. Recombination current is proportional to the base charge density. Injection inefficiency currents are proportional to the charge density at the edges of the base.
4. The emitter is equipotential.
5. Charge storage in the emitter and collector is not important compared to that in the base.

The transistor is assumed to be operating in the grounded emitter configuration with $V_B(x)$ and $V_C(x)$ the voltages at various points in the base and in the collector at the edge of the junction. Let $Q(x)$ be the charge stored per unit length in the base. Then

$$Q = qLW \frac{N_{p1} \exp\left(\frac{qV_B}{kT}\right) + N_{p2} \exp\left[\frac{q(V_B - V_C)}{kT}\right]}{2} \qquad (A.1)$$

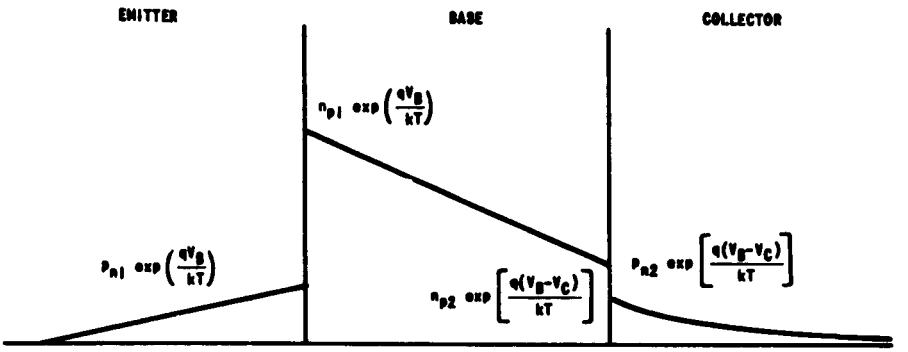
where W is the base width and L is the effective length of the emitter.

The recombination current is given by

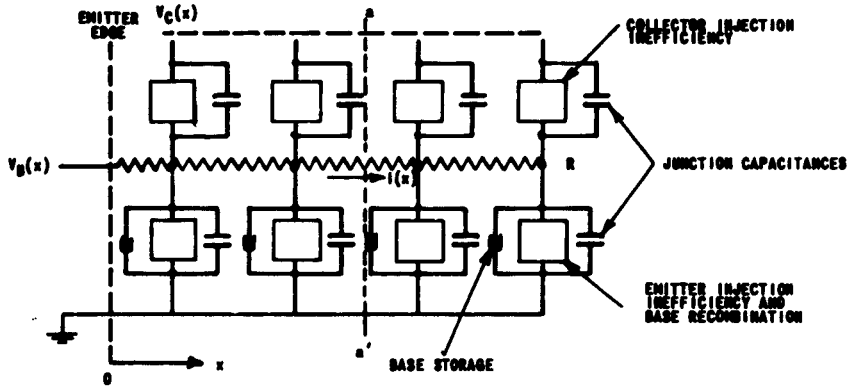
$$I_{rec} = k_1 Q \qquad (A.2)$$

The total current injected by the base into the emitter and collector is

$$I_{inj} = k_2 N_{p1} \exp\left(\frac{qV_B}{kT}\right) + k_3 N_{p2} \exp\left[\frac{2(V_B - V_C)}{kT}\right] \qquad (A.3)$$



a. Minority carrier density at some cross section (e.g., at a - a′)



b. Open-end transmission line, including forward-biased effects

FIG. 60. TRANSISTOR MODEL FOR THE COMPLETE DIFFERENTIAL EQUATION.

The differential equations of the line are

$$\frac{\partial V_B}{\partial x} = -\frac{R}{X} I \qquad \text{or} \qquad \frac{\partial I}{\partial x} = -\frac{X}{R}\frac{\partial^2 V_B}{\partial x^2} \tag{A.4}$$

and

$$\frac{\partial I}{\partial x} = -I_{rec} - I_{inj} - \frac{\partial Q}{\partial t} - \frac{C_E}{X}\frac{\partial V_B}{\partial t} - \frac{C_{CI}}{X}\left(\frac{\partial V_B}{\partial t} - \frac{\partial V_C}{\partial t}\right) \tag{A.5}$$

When the substitutions are made, the complete differential equation becomes:

$$-\frac{X}{R}\frac{\partial^2 V_B}{\partial x^2} = -\frac{k_1 qLW}{2}\left\{N_{p1}\exp\left(\frac{qV_B}{kT}\right) + N_{p2}\exp\left[\frac{q(V_B - V_C)}{kT}\right]\right\} k_2 N_{p1}\exp\frac{qV_B}{kT}$$

$$- k_3 N_{p2}\exp\left[\frac{q(V_B - V_C)}{kT}\right] - \frac{qLW}{2}\left[\frac{qN_{p1}}{kT}\exp\left(\frac{qV_B}{kT}\right)\frac{dV_B}{dt}\right.$$

$$\left. + \frac{qN_{p2}}{kT}\exp\left(\frac{qV_C}{kT}\right)\frac{dV_C}{dt}\right] - \frac{A_E}{X(0.8 - V_B)^{0.37}}\frac{\partial V_B}{\partial t}$$

$$- \frac{A_{CI}}{X(V_C - V_B + 0.8)^{0.37}}\left(\frac{\partial V_B}{dt} - \frac{\partial V_C}{\partial t}\right) \tag{A.6}$$

This equation is so complex that no attempt has been made to solve it. It is presented here for reference, only.

APPENDIX B. CIRCULAR RC TRANSMISSION LINE

If the emitter is circular rather than a long narrow stripe, the following analysis is applicable. Let x represent the distance from the center of an emitter of radius X as shown in Fig. 61. Let the base

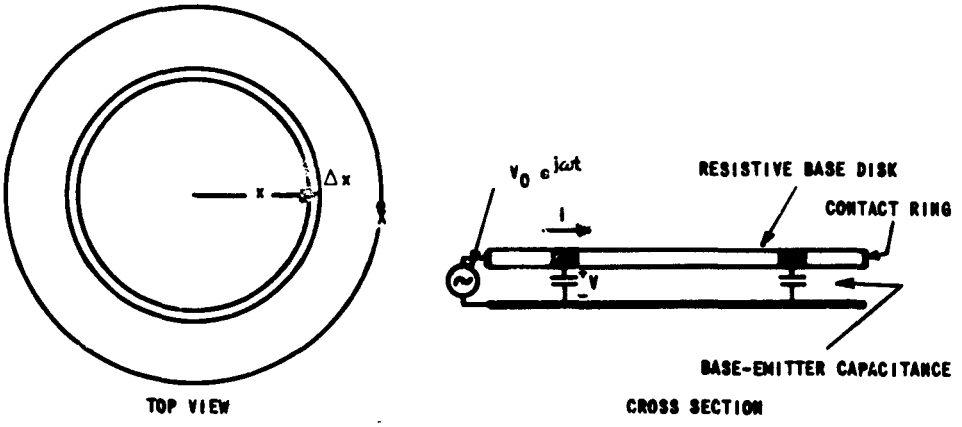


FIG. 61. CIRCULAR EMITTER GEOMETRY.

sheet resistivity be ρ' ohms (per square), and the total shunt capacitance be C. Because of symmetry, currents flow radially only. Let I be the total current flowing radially inward at a distance x and let V be the voltage there. The differential equations are

$$\frac{\partial V}{\partial x} = I \frac{\rho'}{2\pi x} \tag{B.1}$$

or

$$\frac{\partial I}{\partial x} = \frac{2\pi}{\rho'} \frac{\partial\left(x \frac{\partial V}{\partial x}\right)}{\partial x} \tag{B.2}$$

and

$$\frac{\partial I}{\partial x} = \frac{\partial V}{\partial t} \frac{2x}{X^2} C \tag{B.3}$$

Combining these gives the following partial differential equation for the voltage.

$$\frac{\partial^2 V}{\partial x^2} + \frac{1}{x}\frac{\partial V}{\partial x} = \frac{\rho' C}{\pi X^2}\frac{\partial V}{\partial t} \tag{B.4}$$

Consider only the steady-state solution to a sine wave of voltage $V_0 e^{j\omega t}$ applied at $x = X$. Assume $V = V_1(x)e^{j\theta(x)}e^{j\omega t}$ and substitute into (B.4). After simplification this yields the ordinary differential equation

$$\frac{d^2(V_1 e^{j\theta})}{dx^2} + \frac{1}{x}\frac{d(V_1 e^{j\theta})}{dx} - j\omega\frac{\rho' C}{\pi X^2}(V_1 e^{j\theta}) = 0 \tag{B.5}$$

This form of Bessels equation has solutions which are conveniently written as the following,

$$V_1 e^{j\theta} = A\left(\text{ber}\,\frac{x}{L} + j\,\text{bei}\,\frac{x}{L}\right) + B\left(\text{ker}\,\frac{x}{L} + j\,\text{kei}\,\frac{x}{L}\right) \tag{B.6}$$

where

$$L = \sqrt{\frac{\pi X^2}{\omega c \rho'}} \tag{B.7}$$

and ber, bei, ker, and kei are tabulated Bessel functions. Applying the boundary conditions

$$\left.\frac{d(V_1 e^{j\theta})}{dx}\right|_{x=0} = 0 \tag{B.8}$$

and

$$\left.V_1 e^{j\theta}\right|_{x=X} = V_0 \tag{B.9}$$

results in

$$V_1 e^{j\theta} = V_0\frac{\text{ber}\,\frac{x}{L} + j\,\text{bei}\,\frac{x}{L}}{\text{ber}\,\frac{X}{L} + j\,\text{bei}\,\frac{X}{L}} \tag{B.10}$$

The magnitude of Eq. (B.10) is V_1.

$$V_1 = V_0 \sqrt{\frac{\left(\text{ber}\,\frac{x}{L}\right)^2 + \left(\text{bei}\,\frac{x}{L}\right)^2}{\left(\text{ber}\,\frac{X}{L}\right)^2 + \left(\text{bei}\,\frac{X}{L}\right)^2}} \qquad \text{(B.11)}$$

The relative voltage magnitude vs distance from the edge is plotted in Fig. 62 for various values of $X/L = \sqrt{\omega C\rho'/\pi}$. Apparently the line

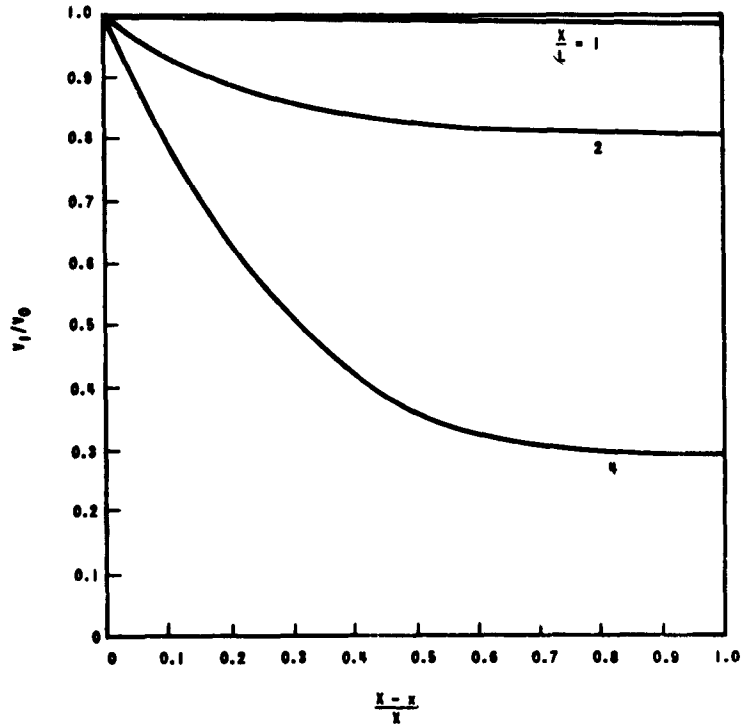


FIG. 62. VOLTAGE VS DISTANCE FROM THE RIM OF A RADIAL RC TRANSMISSION LINE.

cutoff frequency for this case should come from $X/L = \sqrt{\omega C\rho'/2} = 2$, so that

$$f_L = \frac{4}{\pi C\rho'} \qquad \text{(B.12)}$$

The input admittance is

$$Y = \frac{I(X)}{V(x)} = \frac{\frac{2\pi X}{\rho'} \left.\frac{\partial V}{\partial x}\right|_{x=X}}{V_0 e^{j\omega t}} \tag{B.13}$$

$$Y_{in} = 2 \sqrt{\frac{\pi\omega C}{\rho'}} \frac{\text{ber}' \frac{X}{L} + j \text{ bei}' \frac{X}{L}}{\text{ber} \frac{X}{L} + j \text{ bei} \frac{X}{L}} \tag{B.14}$$

The normalized admittance is plotted in Fig. 63. At high frequencies the admittance approaches

$$Y \tilde{=} (1 + j) \sqrt{\frac{2\pi\omega C}{\rho'}} \tag{B.15}$$

Since only the edge is effective at high frequency, this can be expressed as admittance per length of emitter edge.

$$\frac{Y}{2\pi X} = (1 + j) \sqrt{\frac{\omega}{2} \frac{C/\pi X^2}{\rho'}} \tag{B.16}$$

In other words, given a certain sheet resistivity and capacitance per unit area, the high-frequency admittance is directly proportional to the length of edge and varies as the square root of frequency. This same formula is obtained from any emitter geometry as long as the emitter-edge radius of curvature is everywhere much larger than L.

The input power to the circular emitter is

$$P = \frac{1}{2} \text{Re } I(0) \overline{V(0)} \tag{B.17}$$

$$= V_0^2 \sqrt{\frac{\pi\omega C}{\rho'}} \frac{\text{ber}\left(\frac{X}{L}\right) \text{ber}'\left(\frac{X}{L}\right) + \text{bei}\left(\frac{X}{L}\right) \text{bei}'\left(\frac{X}{L}\right)}{\left[\text{ber}\left(\frac{X}{L}\right)\right]^2 + \left[\text{bei}\left(\frac{X}{L}\right)\right]^2} \tag{B.18}$$

The normalized power is plotted in Fig. 64.

The effective series resistance at low frequency is found as follows. Here the shunt current density is constant.

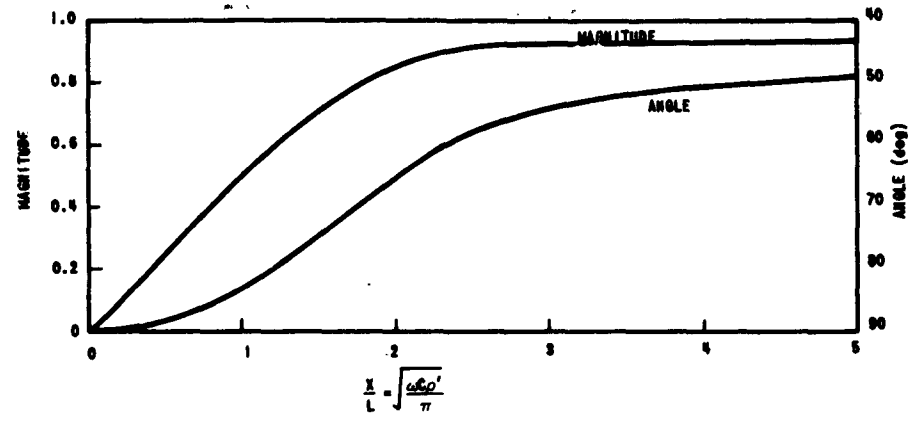


FIG. 63. NORMALIZED INPUT ADMITTANCE $\left(\frac{Y}{2\sqrt{\pi\omega C/\rho'}}\right)$ OF A CIRCULAR RC TRANSMISSION LINE.

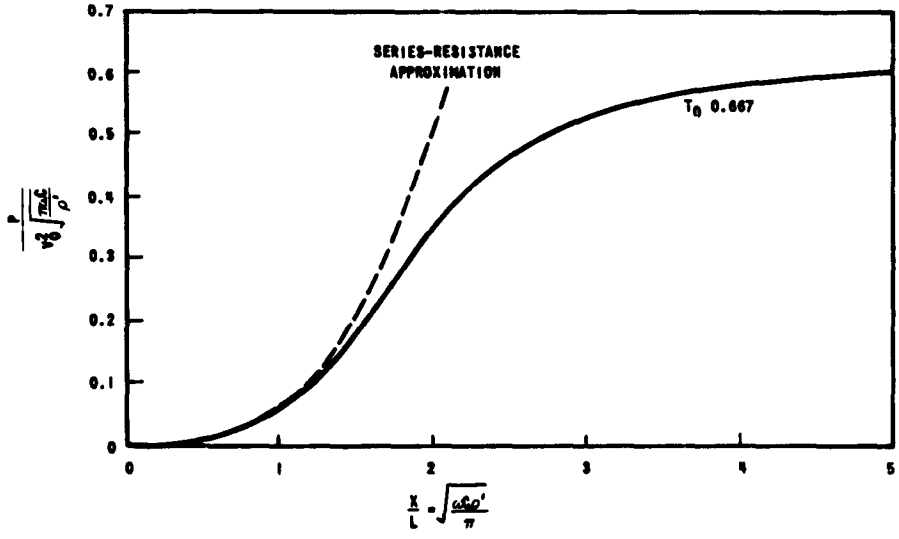


FIG. 64. NORMALIZED INPUT POWER $\left(\frac{P}{V_0^2\sqrt{\pi\omega C/\rho'}}\right)$ FOR A CIRCULAR RC TRANSMISSION LINE.

$$J = \frac{2\pi f C V_0^2}{2\pi X^2} = \frac{f C V_0^2}{X^2} \tag{B.19}$$

The radial current is therefore

$$I = \frac{f C V_0^2}{X^2} \pi x^2 \tag{B.20}$$

The radial resistance of a segment dx is

$$R_x = \rho' \frac{dx}{2\pi x} \tag{B.21}$$

The total power is therefore

$$P = \int_0^X I^2 R_x dx = \int_0^X \left(\frac{\pi f C V_0^2}{X^2}\right)^2 \frac{\rho'}{2\pi} x^3 dx = \left(\frac{\pi f C V_0^2}{X^2}\right)^2 \frac{\rho'}{2\pi} \frac{X^4}{4} \tag{B.22}$$

The total power is also

$$P = \left(\frac{V_C}{\sqrt{2}} 2\pi F C\right)^2 R \tag{B.23}$$

so that equating the last equations and solving for R, the effective series resistance gives

$$R = \frac{\rho'}{8\pi} \tag{B.24}$$

It is interesting to see how much error in computing power results from assuming that the total current is merely the applied voltage divided by the total shunt reactance and that the power is I^2R. When the power is normalized in the same way and plotted in Fig. 64, the error is shown to be

$$\begin{aligned} &23\% \text{ when } \sqrt{\frac{\omega C \rho'}{\pi}} = 1.7 \\ &7.5\% \text{ when } \sqrt{\frac{\omega C \rho'}{\pi}} = 1.4 \end{aligned} \tag{B.25}$$

APPENDIX C. APPLICATION OF LINEAR RC LINE THEORY TO INTERDIGITATED EMITTER-BASE GEOMETRY

When other than the linear or circular geometry is encountered it is possible to approximate the actual geometry by combinations of linear or circular lines. For example, the TA2084 and SN102 transistors have the structure shown in Fig. 4. An approximation to this structure is a parallel combination of two linear emitters as shown in Fig. 65. Here

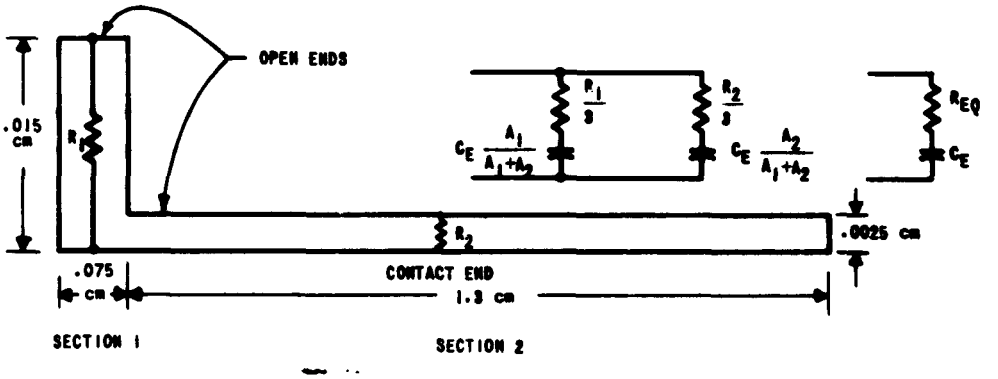


FIG. 65. APPROXIMATE RC LINE GEOMETRY AND LOW-FREQUENCY EQUIVALENT CIRCUIT FOR INTERDIGITATED TRANSISTOR.

the short wide element represents the finger cut in the center and laid out flat. The line length is one-half the emitter finger width and the line width is the total finger edge. The long narrow element represents the emitter lead contact area. Its length is the depth of the contact area and its width is the total exposed edge at the throats of the fingers and the sides of the contact area.

Let R_1 and R_2 be the resistances of the two sections, and A_1 and A_2 be their areas. Let ρ' be the base sheet resistivity which is the same for both sections, and C_E be the total shunt capacitance. Then from the dimensions given,

$$R_1 = \rho' \frac{0.015}{0.075} = \frac{\rho'}{5} \tag{C.1}$$

$$R_2 = \rho' \frac{0.0025}{1.3} = \frac{\rho'}{520} \tag{C.2}$$

The low-frequency equivalent circuit is also shown in Fig. 65. If the power in the two-branch circuit is equated to that in the single-branch circuit, we obtain

$$R_{EQ} = \frac{R_1}{3}\left(\frac{A_1}{A_1 + A_2}\right)^2 + \frac{R_2}{3}\left(\frac{A_2}{A_1 + A_2}\right)^2 \tag{C.3}$$

When the values are substituted, this gives

$$\rho' = 130\, R_{EQ} \tag{C.4}$$

Measurements on the TA2084 transistor gave $C_E = 400$ pf and an input series resistance of 19Ω at low frequency, decreasing to 3Ω at high frequency. Therefore $R_{EQ} = 16\Omega$ and

$$\rho'_{TA2084} = 2080\Omega, \qquad R_1 = 416\Omega, \qquad R_2 = 4\Omega \tag{C.5}$$

The line cutoff frequency for section 1 is

$$f_{L1} = \frac{A_1 + A_2}{\pi R_1 C_E A_1} = 7.4 \text{ Mc} \tag{C.6}$$

The equivalent circuit can be given in three frequency regions as shown in Fig. 66. The low-frequency circuit applies up to about half the first cutoff frequency. The complete two-emitter circuit then applies up to about four times the first cutoff frequency. Past this point there is very little voltage reaching the rear part of section 1 so the assumption is made that its length is the same as section 2 and the two sections are combined. The cutoff frequency of this line is

$$F_{L2} = 268 \text{ Mc} \tag{C.7}$$

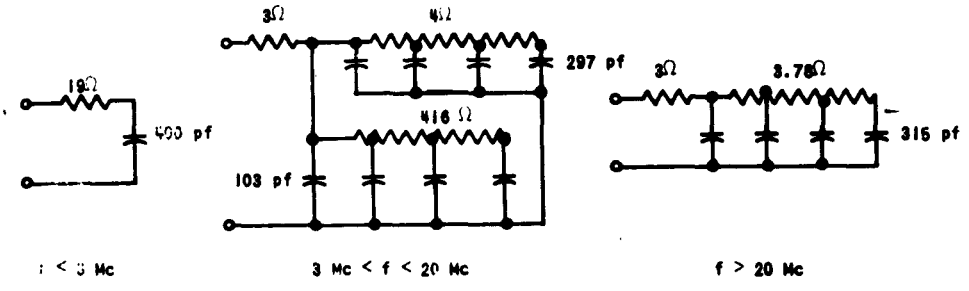


FIG. 66. EQUIVALENT CIRCUITS FOR INTERDIGITATED EMITTER GEOMETRY OF THE TA2084 TRANSISTOR.

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